

5-2001

## Conference of Microelectronics Research 2001

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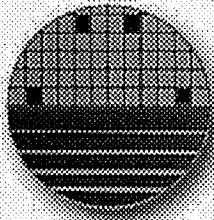
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*Microelectronic Engineering at RIT*  
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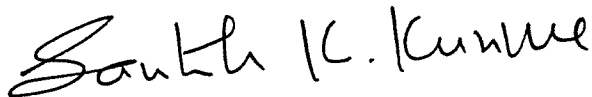
# *Editorial*

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These proceedings contain research papers presented at the 19<sup>th</sup> Annual Microelectronic Engineering Conference held at the Rochester Institute of Technology (RIT) on May 14 through 16, 2001 by senior undergraduate students of Microelectronic Engineering of RIT. The students graduating with BS degree in Microelectronic Engineering are required to take a two course sequence of capstone design courses, EMCR 680 and EMCR 690 entitled Seminar/Research I and II in their fifth year. The first course consists of submission of a research proposal, related to the field of semiconductor devices and processing, by each student. Following the approval of the proposal, the students carry out their projects through the ten-week spring quarter. Toward the end of the spring quarter, the students are required to present their work at the Microelectronic Engineering Conference held at RIT annually in the month of May.

The class of 2001 presented impressive and technically challenging research projects on various topics ranging from advanced microithography, novel device structures and processes, back-end processes, and MEM devices.

I congratulate the students for their valuable contributions to the conference and to the Microelectronic Engineering at RIT. On behalf of the faculty and staff of the Department of Microelectronic Engineering, I wish the students success in their career ahead.



**Dr. Santosh Kurinec**

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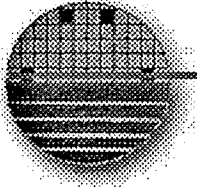
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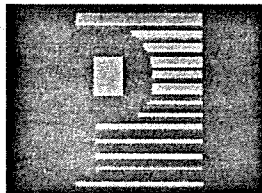
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# **19<sup>th</sup> Annual Microelectronic Engineering Conference**

Kate Gleason College of Engineering  
Rochester Institute of Technology  
Rochester, NY 14623

May 14-16, 2001

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# Evaluation of Source Geometry Using a Pinhole Camera

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**Abstract** -- A pinhole camera was used to evaluate source geometry of the GCA6700 g-line stepper. To create the camera, a photomask with various pinhole sizes was placed in the stepper, in close proximity to a wafer to generate an image. The images were evaluated to determine the shape and observe the radial intensity of the source. The variation across the source was evaluated because varying intensity across the wafer results and contributes to changes in critical dimension. Dose was varied in order to show how an illumination source might be characterized. As dose increased, the pinhole image became larger. Stacking the images could be used to create a three dimensional image of the source. Additionally, source images were used to verify the numerical aperture of the condenser lens of the illumination system.

## 1. INTRODUCTION

Knowledge of illuminator geometry is important in achieving optimum performance from optical tools. Illumination source geometry is used to measure telecentricity error effects, effective source shift, and resulting changes in intensity across the wafer.

Telecentricity is when the chief rays of an optical system are collimated, meaning the chief rays are parallel to the optical axis [1].

An illumination source can shift so that it is not in direct alignment with the pupil of our lens system. The illuminator system is designed to align with the lens system, when it may have actually shifted to one side. Some intensity will be lost when the energy falls outside the lens pupil [2].

Changes in intensity across the source are important because this results in changes in intensity across the wafer. This in turn changes linewidths on the wafer, and can be detrimental when printing small gate sizes.

Source imaging with a pinhole camera is a convenient way to observe source geometry using an easily repeated, simple setup. Since the illumination source cannot be inspected by the naked eye, a pinhole camera projects an image of the illuminator onto the wafer surface.

### A. What is a pinhole camera?

The setup for a pinhole camera is shown in Figure 1. A mask with small pinhole causes an image of the source to appear in resist on the wafer. The pinhole in a pinhole camera acts as the lens. The pinhole forces every point emitting light from the source to form a smaller point on the wafer, so the image is crisp. This method requires longer exposure time than imaging with a lens. Conventional camera lenses allow a much larger hole to admit light, and therefore have faster exposure time. [3]

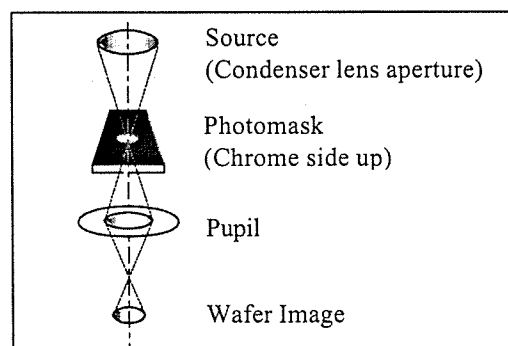


Figure 1: General Pinhole Camera Setup

## 2. EXPERIMENT

In this experiment, source geometry of the GCA 6700 436 nm G-line stepper was evaluated using a pinhole camera. A dark field mask was designed with pinholes varying in size from 50 – 600  $\mu\text{m}$ . The mask was created using the MEBES III electron beam mask making system. The illumination source was imaged in one  $\mu\text{m}$  thick Shipley 812 photoresist on p-type wafers. HMDS (hexamethyl-disilazane) adhesion promoter was used before the resist coat. Small pellicle rings were used to attach the wafer in close proximity to the photomask. Table 1 shows the source imaging process steps. CD-26 developer was used in the develop step.

Table 1: Process Steps for Pinhole Imaging

Step	Time (sec)	Temp (°C)
Dehydration Bake	120	200
Coat (4500 RPM)	60	
Prebake	120	90
Expose	30	
Post-Exposure Bake	45	115
Develop	50	
Hardbake	160	120

### A. Setup

Normally, a stepper setup from top to bottom begins with the source, then condenser lens, photomask, objective lens, and finally, the wafer. Figure 1 illustrated the standard setup. In this experiment, imaging was done at the mask plane, above the objective lens. This way, there were no aberrations from the objective lens to deal with.

The wafer was attached to mask using a small pellicle ring. When illumination travels through the objective lens, the area exposed at the wafer plane is 5x5 times smaller than the area at the mask stage, so the intensity is 25 times higher at the wafer stage. Since all imaging was done at the mask plane, wafers were exposed 25 times longer than in standard processing. The wafers were exposed manually using the 436nm source of the GCA 6700 G-line stepper. Figures 2a and 2b show the experimental setup.

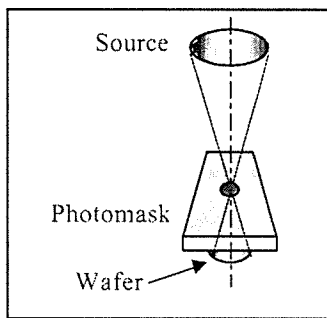


Figure 2a: Experiment Setup

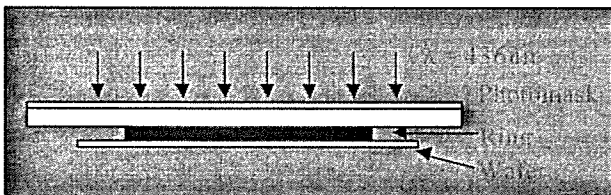


Figure 2b: Setup at Mask Plane

### B. Exposure Dose Variations

The source was imaged at various exposure doses to observe the possibility of three-dimensional source imaging. The intensity measured at the mask was 7.0 mW/cm<sup>2</sup>. The dose, D, was found by multiplying the intensity, I, by the time, t, in seconds, as shown in the following equation. Table 2 shows resulting dose for each wafer.

$$D = I * t \quad (1)$$

Table 2: Varied Exposure Dose Values

Wafer	Intensity (mW/cm <sup>2</sup> )	Exposure Time (sec)	Dose (mJ/cm <sup>2</sup> )
M1	7.0	30	210
M2	7.0	25	175
M3	7.0	20	140
M4	7.0	15	105
M5	7.0	10	70
M6	7.0	5	35

### C. Beam3 Simulations

Beam3 software was used to determine the theoretical numerical aperture of the condenser lens. The mask was placed 2700 μm from the source in the simulation. The mask thickness was 3000 μm. A ray was placed 460 μm above the optical axis, creating a half angle of 9.67° with the pinhole center. The ray reached the wafer at 1300 μm below the optical axis. As the pinhole size increased, the distance from the incident ray on the wafer from the axis was 1300 μm added to the radius of the pinhole. This accounts for some variation in experimental calculation of the numerical aperture of the condenser lens.

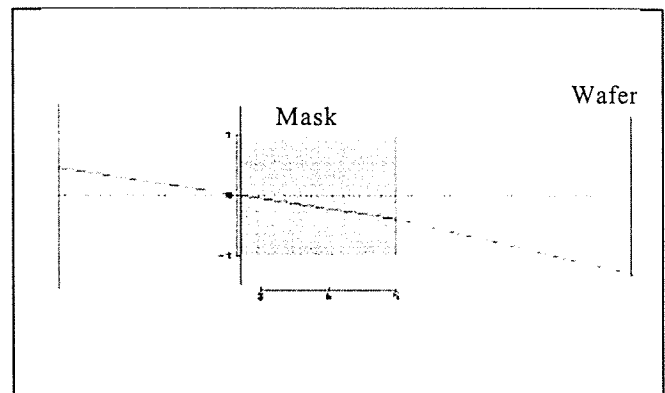


Figure 3: Beam3 Simulation

### 3. RESULTS AND ANALYSIS

#### A. Source Images

Images of the source are shown in Figure 4. It is evident that intensity drops off radially for each image. The source shapes in Figure 4 were projected through a 300 $\mu$ m pinhole to form resist images. To create each image, the exposure dose was increased. The varied exposure dose from Table 2 was used to get an idea of what a three-dimensional source image would look like. Variations in radial intensity, though less of a threat than asymmetry, could have an effect on printable critical dimension. Figure 5 shows negligible asymmetry in the images, and any questionable effects were the result of standing waves in the resist.

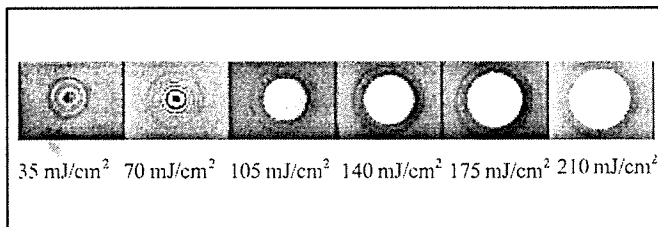


Figure 4: Images of 300 $\mu$ m Pinhole with Varied Exposure Dose

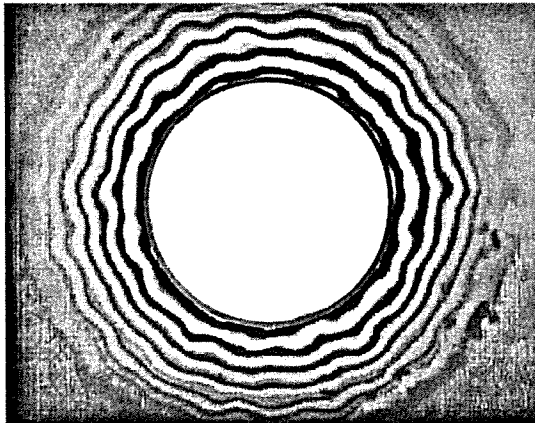


Figure 5: Symmetrical Pinhole Shape

#### B. Three-dimensional Source Images

Dose was varied from 35mJ/cm<sup>2</sup> to 210mJ/cm<sup>2</sup>, effectively changing the image of a 300 $\mu$ m pinhole, as seen in Figure 4. Stacking the images on top of one another can be used to produce a three-dimensional effect,

as seen in Prolith source images. Software is available to create the three-dimensional images to help in characterizing sources. Just as lenses are characterized, source characterization is an important way to evaluate tool capabilities.

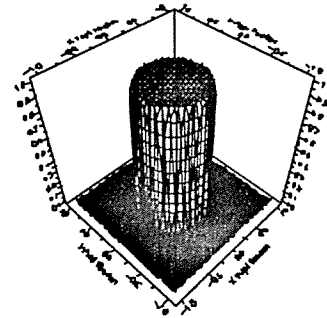


Figure 6: Prolith 3-dimensional Source Image

#### C. NAc Measurement

The pinhole images were used to verify the Numerical Aperture of the condenser lens. Figure 7 demonstrates the angles and measurements used in the calculations. The angle at the mask is equal to the angle formed by the condenser lens. The numerical aperture is the sine of the half angle the incident light makes as it reaches the quartz through the pinhole. Theoretically, the numerical aperture should be 0.16. Experimental measurements gave a numerical aperture of 0.14, about 12.5% error. This error is due to the threshold of the resist, exposure time, and size of the pinhole.

Theoretical:

$$NA_c = NA_o * \text{partial coherence} \quad (2)$$

$$NA_c = \sin \alpha = 0.16$$

Experimental

$$a^2 + b^2 = c^2 \quad (3)$$

$$NA_c = \sin \alpha = a / c \quad (4)$$

$$NA_c = 0.14$$



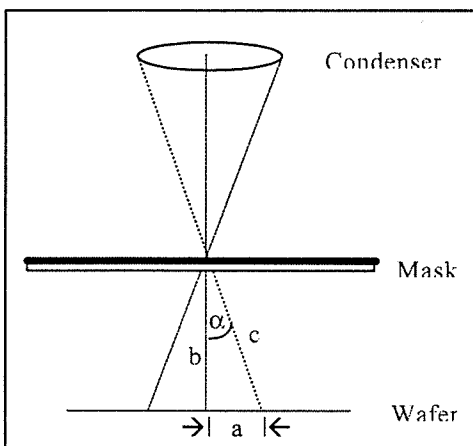


Figure 7: Prolith 3-dimensional Source Image

#### 4. CONCLUSION

Evaluation of source geometry has a definite benefit to industry. Using a pinhole camera, source geometry can be determined easily and conveniently. The projected image shows any irregularities in intensity distribution. As previously mentioned, imperfect source geometry accounts for across chip linewidth variations, and partial coherence variations. Another type of pinhole that may be used is a diffraction grating pinhole, often used in experiments to determine effective source shift [4].

Future work may include many quantitative experiments, such as source shift measurement, telecentricity error measurement, and Fourier Transform evaluation of images. A BARC should be used to eliminate standing waves in the resist. It would also be beneficial to perform the experiment with I-line, Deep UV, and off-axis illumination sources.

#### REFERENCES

- [1] J. Michalski, "What Is Telecentricity?" Edmund Industrial Optics, 2001. Retrieved May 14, 2001, from the World Wide Web: <http://www.edmundoptics.com/techsup/tsb/telecentricity.cfm>
- [2] K. Sato, S. Tanaka, T. Fujisawa, and S. Inoue, SPIE Vol. 3679, p. 99, 1999.
- [3] M. Brain, "How does a pinhole camera work?" 1998-2001. Retrieved April 27, 2001, from the World Wide Web: <http://howstuffworks.lycos.com/question131.htm>
- [4] J. Kirk, C. Progler, "Pinholes and Pupil Fills," Microlithography World, Autumn 1997.

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**Marilyn Maloney**, originally from Buffalo, NY, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2001. She attained co-op work

experience at Photonics Inc. and Motorola Inc. She is joining Motorola Corporation as a lithography engineer starting July 2001.

# i-line Resist Process Monitor

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**Abstract--** In order to confidently reproduce results obtained from experimentation or standard processing, the stability of the involved equipment's performance must be understood. Therefore, it is important to monitor, on a regular basis, the outputs of an equipment set which are delivering a desired process. In this paper, a qualification test or "qual" will be defined for RIT's 150mm i-line photolithography process which utilizes a Canon FPA 2000-i1 exposure tool.

## 1. INTRODUCTION

Currently RIT utilizes a g-line(436nm) lithography process for fabrication of devices with minimum feature sizes of 1 $\mu$ m. Recently, a Canon FPA 2000 i-1 stepper was donated to RIT. Transitioning to an i-line(365nm) process will enable research and academic instruction in sub-micron devices. This new capability for RIT is predicted by Rayleigh's formula for projection optics as follows:

$$R = k_1 \frac{\lambda}{NA}$$

where  $k_1$  is the process factor, typically  $\approx 0.7$ ,  $\lambda$  is the illumination source wavelength = 365nm for i-line, and NA is the numerical aperture of the system, which is 0.52 for this Canon stepper. With these values, the minimum feature size, R, is approximately 0.5 $\mu$ m.

This sub-micron capability has the consequence of smaller process windows. Therefore it is import to understand and monitor the parameters associated with producing 0.5 $\mu$ m features. This report will define a series of tests to monitor the parameters associated with reproducing sub-micron features consistently. A procedure for performing these tests, not included in this report, will be place in the clean room for reference.

## 2. CHARACTERISTICS

The practice of monitoring the performance of a piece of equipment or process is commonly referred to as a qualification, or "qual." A qual is performed on some interval found to be representative of the typical

performance associated with a tool or process. In this case, the qual was performed on a daily basis. For this qual the following parameters were monitored for RIT's i-line resist process:

### A. Hg-arc lamp intensity & field uniformity

The Hg(mercury)-arc lamp is the illumination source used in the stepper. There are several peaks in the Hg spectrum as shown in figure 1. The Canon FPA 2000 i-1 stepper is tuned to utilized the i-line peak at 365nm. The lamp intensity is monitored to understand the lifetime limitations of the light source. Although the lamp lifetime is specified as 1,500 hours of use, expenses to RIT can be reduced by monitoring the performance of the lamp and replacing it only as necessary based on process monitor data. Measurement of the lamp intensity is a utility performed using Canon's AUX IUC command.

### B. Resist thickness

Prior to lithographic patterning, the wafers are coated with photoresist. The thickness of photoresist is optimized based on the requirements of the pattern imaging, etch selectivity, and implant blocking. Therefore, it is important to monitor the thickness of the resist coating process, and determine if the variation is acceptable based on the requirements above. For the resist thickness monitor, the resist is measured on five locations(fig. 2) on the coated wafer using the Nanometrics Nanospec AFT-200.

### C. Ambient environmental conditions

Lithography is one of the few process in the fab where the wafers are processed out in the open. As such, the resist coating process, and to a lesser extent, the resist-exposure reaction are sensitive to fluctuations in the temperature and the humidity of the fab environment. Although there is no immediate control of these conditions, monitoring the temperature and humidity will allow correlations to be made regarding the impact of environmental conditions on the resist process. To monitor temperature and humidity in the fab, a digital

thermometer/hygrometer was mounted near the wafer track.

#### *D. Stepper focus*

Optimum focus is crucial to lithographic imaging. For a given device level, a focus setting is defined as an offset from the stepper system focus. By monitoring the stepper system focus, the accuracy of offset focus values can be ensured. Focus is determined as a result of exposing the coated wafer using the qual job. The focus evaluation array is located on the right side of the wafer. The focus job creates a "Christmas tree" pattern by exposing a  $0.5\mu\text{m}$  grating through a matrix of focus & exposure values. The location of the peak of the "Christmas tree" indicates a focus correction whereby right of center is a positive correction and left of center is a negative correction. See fig. 3.

#### *E. Dose to Clear ( $E_0$ )*

The dose to clear or  $E_0$  value is the exposure energy at which an open exposure field is completely cleared of resist. This value is sensitive to the interaction of the resist and developer chemistries and will be indicative of instability elsewhere in the process. The  $E_0$  array is located on the left side of the wafer. Fig 3 shows the qual wafer layout and indicates specific  $E_0$  dose values.

#### *F. Critical dimension (CD)*

The  $0.5\mu\text{m}$  CD feature is the primary parameter of interest in the i-line resist process. This might be the only lithographic parameter(excluding overlay) monitored during semiconductor and microsystems device fabrication. By monitoring the CD performance regularly as part of the qual, the history collected will allow for process excursions to be investigated and correlated to other parameters. The CD pattern is imaged on the qual wafer using the Canon 365 reticle. The  $0.5\mu\text{m}$  lines are then measured at five locations on the wafer as shown in fig. 3. The measurements are made using the Hitachi S-6780 CD-SEM.

#### *G. Data logging*

The data tracking system in use at RIT, MESA, allows only for lot data to be entered. At this time, equipment related data can not be tracked in MESA. Also, there are no other statistical packages available in the clean room to allow equipment data tracking. Therefore, paper logs are being used to track the data. A blank log sheet is shown in fig. 4. The raw data measurements are hand written at the bottom of the screen and then a data point is hand plotted on the graph above. Each data point is then connected to

form a trend chart. These logging sheets will be posted at each machine for ease of view ability.

### 3. RESULTS AND DISCUSSION

The qual was run and data collected on a daily basis from April 16 through May 4. Data points were logged once a day, except for April 20, where a continuous run of 7 wafers was performed in order to get an idea of wafer to wafer stability. Because of the small number of data points collected, statistical parameters were not calculated at this time.

Fig. 5 shows the temperature and humidity of the fab environment. Alone, this graph does not indicate anything except how well the building's environmental controls operate. However, when correlated to the resist thickness performance shown in fig. 6, there is evidence that fab environmental controls may need to be improved. This is further evidenced in fig. 7, where the  $E_0$  variation appears to show correlation to resist thickness variability that resulted from the instability in environmental conditions. Fig. 8 shows the  $0.5\mu\text{m}$  CD performance. For this graph, only the stability between measurement is meaningful. The optimum dose to size the  $0.5\mu\text{m}$  lines was not used because the CD-SEM was inoperative during the data collection portion of this project. All wafers were run at a dose of 150mj, and were stored until the SEM was available for measurements. Fig. 9 shows the performance of the focus test. This parameter, while not controllable must be track and corrected at every excursion. The last qual graph is the Hg-arc lamp intensity shown in fig. 10. Again this parameter is not controllable. This graph is used to track to lamp life time. As the lamp ages, the intensity degrades. Although the Canon specification for minimum lamp intensity is  $600\text{mW}/\text{cm}^2$ , for RIT budget reasons the lamp is run until lithographic performance degrades.

### 4. CONCLUSION

In this project, a series of qualification tests have been established. Regular monitoring of these qual results will allow the performance and capability of RIT's i-line lithography process to be understood. As more data is collected, statistical parameters can be calculated such as control limits and capability indices. Additional future projects relating to this work should include stepper overlay and stage precision monitoring, migration of data collection to MESA, similar testing for the g-line and DUV process, and continuous process improvement.

### ACKNOWLEDGMENTS

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## HIGH PRESSURE MERCURY VAPOR LAMP

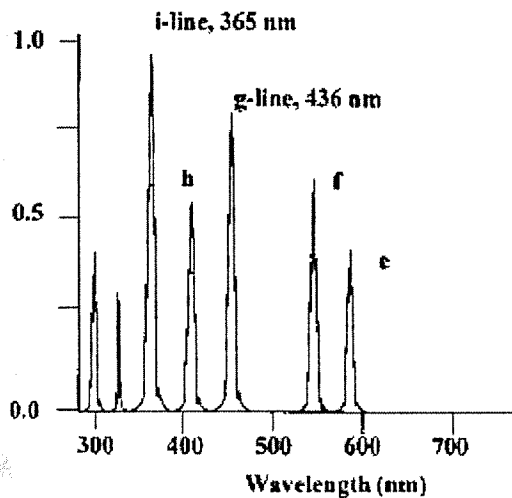


Fig. 1

### Resist Thickness Measurement Locations

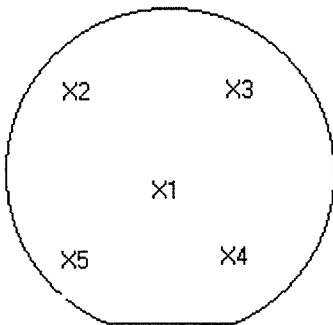


Fig.2

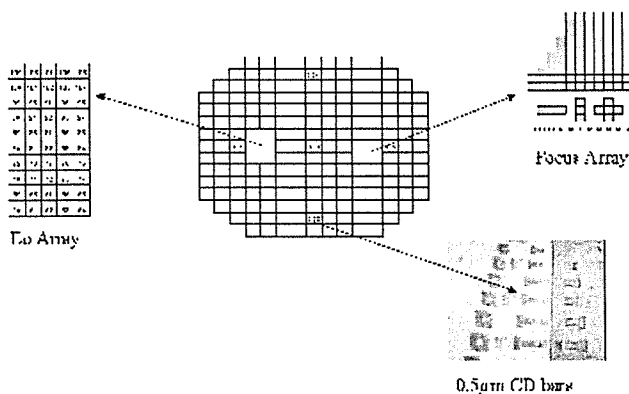


Fig.3 Qual Wafer Layout

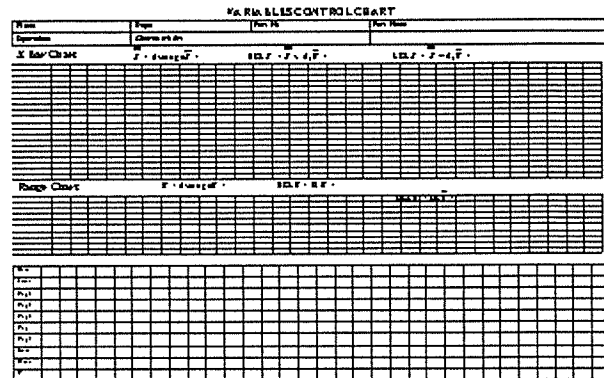


Fig.4 Blank Data sheet

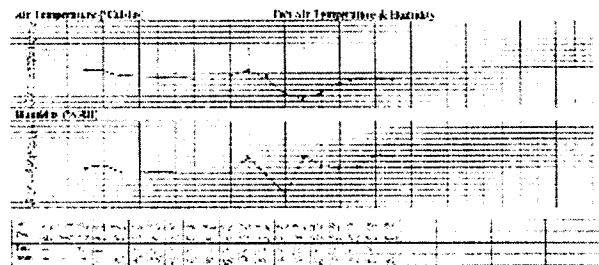


Fig. 5 Fab Temperature & Humidity

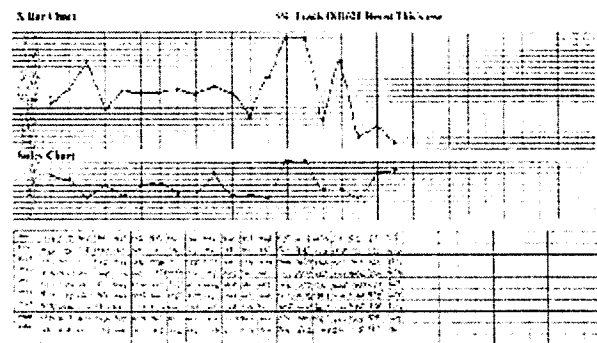


Fig. 6 Resist Thickness & Stdev.

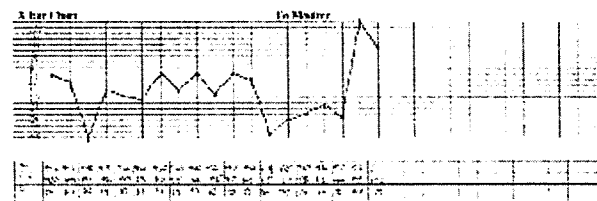


Fig. 7 Eo Monitor

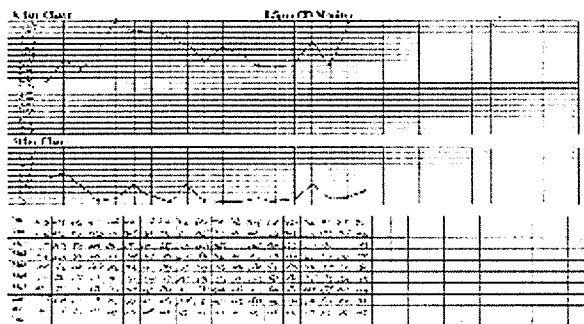


Fig. 8 0.5 $\mu$ m CD Monitor

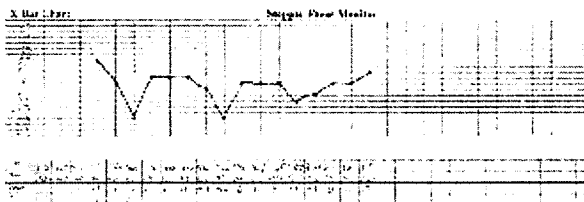


Fig. 9 Stepper Focus Monitor

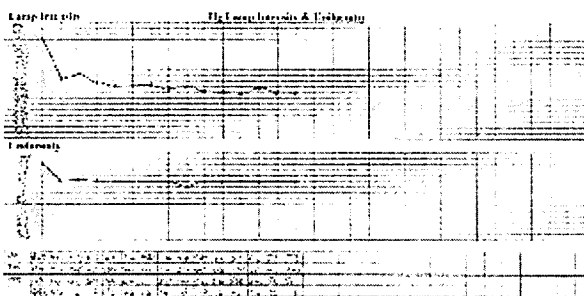


Fig. 10 Hg-arc Lamp Intensity & Uniformity

# Development of Automated Alignment Methodology on the Canon I-line Stepper

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**Abstract --** Lithography is one of the most crucial processes that is used in modern integrated circuit (IC) fabrication. Level to level alignment and overlay measurements are key factors within lithographic processes. A stepper with an automated level to level alignment system can significantly improve wafer throughput and therefore increase profit for a company. There are many factors that can either enhance or hinder a tool's ability to align one level on top of another. For the past couple of years, RIT has had a Canon FPA 2000 i1 I-line stepper in their possession and the automated alignment system has never been utilized, until now. The data that proves this particular tool can and will align levels automatically is shown throughout. Some of the issues that arose throughout the study will also be discussed.

## 1. INTRODUCTION

One of the most critical areas of any integrated circuit (IC) production facility is microlithography. Within microlithography, there are two very important factors. These two factors are alignment and overlay measurement. Alignment is defined as "the process of determining the position, orientation, and distortion of the patterns already on the wafer and then placing them in the correct relation to the projected image"[1]. "Overlay" can be defined as "how accurately each successive patterned layer is matched to the previous layers" [1]. Both of these steps are usually carried out by optical means. As our technology improves to smaller and smaller critical dimensions (CDs) our tools will have to change and we may not be using optical exposure tools anymore. This implies that our alignment systems will also have to change with the new technology. Also, as our CDs have gotten smaller, so has overlay budget. Overlay was typically measured on an optical microscope. Now with our smaller overlay tolerances, the overlay will be measured on Scanning Electron Microscopes (SEMs). Current CDs are being measured in this way.

There are two main types of alignment that are currently being used. Both are types of alignment on optical exposure tools can be done using alignment

sensors. The first, "global" alignment, is probably more utilized throughout industry than the second, "field-by-field." This is because the global alignment procedure is much quicker than the "field-by-field" approach. Global alignment does not locate all the fields on the wafer. Also, the global alignment uses a "best overall fit" approach, which makes it less sensitive to noise. The "field-by-field" approach will collect data from one field at a time to align only that field. This makes the alignment sensitive to the optomechanical stability of the tool.

The alignment process itself can be broken down into two steps; coarse, alignment and fine alignment. During the coarse alignment process, the alignment mark must be within several hundred microns in order for the alignment sensor to "capture" the alignment target. The wafer will then be adjusted so that the alignment is within a few microns. This is enough to move the wafer into the range of the fine alignment system. The alignment sensor will then tell the tool to adjust the position of the wafer so that the alignment is less than a micron.

When overlay measurement is discussed, one must understand that we are measuring the difference in position, orientation, and distortion between two consecutive levels of an IC. There are two types of overlay that are typically measured. The first is "tool-to-itself" overlay. This implies that the two levels that are being measured were both exposed on the same tool. The other type of overlay that is measured is called "tool-to-tool" overlay, which is a comparison of two consecutive layers exposed on different tools. There are many structures that can be used to measure overlay. The two most common types are the "box-in-box" structures and the "diamond-in-diamond" structures.

At RIT the Canon I-line Fine Pattern Aligner system has the ability to align one layer on top of another layer. Since the tool has been turned over to RIT, neither the students nor the faculty have actually gotten the system to work properly. However, Advanced Vision Technologies (AVT) has shown that it is possible. The only issue is that confidence in the tool has never been established. This is one of the key issues that must be addressed. Also, it was shown that the overlay capabilities of the tool are less than 1  $\mu\text{m}$ . This result also needs to be verified and reproduced.

One of the reasons that RIT has not been able to use the tool with the automatic alignment system running is because there are very few RIT reticles with the Canon alignment marks on them. This is another issue that must be addressed in order to get the RIT processes running smoothly on the tool.

There is a second issue that has caused some trouble with the alignment system. This is the lamp intensity. The current lamp is degraded to a point where the alignment system cannot work properly. All the key issues that hinder the ability to align properly must be addressed prior to the start of the investigation.

## 2. PROCEDURE

For the purpose of conducting this experiment, the following procedure was followed. The Canon stepper is only capable of processing 6 inch wafers, so these were obtained. To start, a thermal oxide was grown on the surface of the silicon substrate. This oxide was approximately 500 Å thick. This was done using recipe 250 on the Bruce Furnace. To check the uniformity across the wafer and also wafer-to-wafer uniformity, 3 wafers were measure at 5 different locations on the surface.

Using the coat recipe on the SSI 6 inch wafer track, the wafers were coated with approximately 1 µm of OiR 620 I-line resist. As part of this standard process, there is a dehydration bake and vapor prime of hexamethyldisilazane (HMDS) at 125° C and a pre bake at 90° C.

After the first coat of resist, the exposure is done. This is done using the first level alignment reticle from Advanced Vision Technologies (AVT). The energy used for the exposure was 150 mJ/cm<sup>2</sup>. The focus setting was kept at 0 µm throughout the study.

After the exposure, the image must be developed. The development process is also a standard procedure on the SSI wafer track. It consists of a post bake at 110° C. After the MF CD-26 developer is dispersed and the wafer is then rinsed with deionized water, the wafer moves into another oven for the hard bake at 120° C.

Now the image must be transferred from the resist to the oxide. This is done using the FACOXIDE recipe on the Drytek Quad in the RIT Fab. This recipe utilizes standard SF<sub>6</sub> and CHF<sub>3</sub> chemistry. The SF<sub>6</sub> flows into the chamber at a rate of 20 sccm. The CHF<sub>3</sub> flows into the chamber at a rate of 40 sccm. The power used during the etch process is 250 W. The pressure was set to 270 mTorr. The total etch time per wafer was approximately 2 minutes and 15 seconds. The etch rate using this recipe is approximately 250 Å per minute. Therefore this time allowed for a slight over etch.

Now that there is a permanent first level image etched into the SiO<sub>2</sub>, the second level process can begin. To start the second level process, the OiR 620 resist must

be coated onto the surface of the wafer. This is done using the same coat recipe used before on the SSI wafer track.

With the second coating of resist spread onto the wafer, the second level exposure can begin. This was done using the second level reticle from AVT. This second level exposure utilizes the automated alignment system on the Canon. Once again the exposure energy that was used was 150 mJ/cm<sup>2</sup>.

Now that the resist has been exposed for the second time, it must be developed again. Once again this was done using the develop line on the SSI wafer track. Now that the image can be seen in the resist, the level-to-level overlay can be measured. This was done on an optical microscope using the 1 µm verniers. The overlay was then tabulated.

## 3. RESULTS

The tabulated data was taken from a sample of 9 wafers. A total of 84 measurement points in X and in Y were taken from the 9 wafers. From the first 3 wafers a total of 60 data points were collected. This shows that there were a total of 20 measurements per wafer. This was done to achieve an idea of the uniformity across the wafer. The next 24 measurements came from the remaining 6 wafers. These measurements consisted of 4 sites per wafer, which were taken at the corner die. The corner die correspond to sites 1, 5, 16, and 20 depicted in the wafer map shown below (figure 1). This is the minimum needed to see any wafer rotation. The averages of the data collected are displayed in table 1 shown below.

	X (µm)	Y (µm)
AVG	1.79	0
STD	0.42	0

Table 1: Average of X and Y overlay data

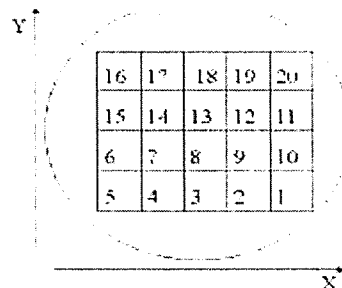


Fig 1: wafer map

## 4. DISCUSSION

The data shown earlier provides evidence of the usefulness of the automated alignment system. When all the pieces to the puzzle fit, the tool is capable of aligning one level on top of another. The data illustrates some kind of offset in the X direction of about +1.8  $\mu\text{m}$ . There seems to be no offset in the Y direction. The X offset could possibly be corrected by "writing" an X offset by -1.8  $\mu\text{m}$ .

There are some other issues that must be taken care of. First, Canon alignment marks must be etched into the reticle. If this is not done prior to processing, there is no chance of alignment. The alignment system will have nothing to align to.

Next, the stepper job must be written so that the stepper is told to align the reticle to the wafer. The stepper job must also have the pattern recognition tolerances set to a reasonable level. If the tolerances are set too high, the tool will not recognize the pattern if there is any small change in the pattern. This will take care of any distortion of the pattern by the etch process. If the tolerances are set too low, any pattern on the wafer may look like the Canon alignment mark. That is why it is crucial to set this tolerance at a reasonable level.

Finally, another tool parameter that must be paid attention to is the lamp intensity. The lamp can play a major role in the ability of the tool to align both the reticle to the column and also the reticle to the wafer. Once the intensity degrades to low, the tool will have trouble aligning the reticle to the column. The reticle will then have to be aligned manually. However, a person will never align the reticle as well as the tool can. This is a major contributor to the overlay error that can be seen. Also, the intensity of the lamp can hinder the ability of the tool to recognize the alignment mark that is needed to align the reticle to the wafer. If this is the case, the tool must be "helped" along using some manual commands. This is actually a semi-automatic alignment process. But it does prove that the tool can utilize this automated alignment system.

## 5. CONCLUSIONS

It has been proven that the Canon FPA 2000 i1 can utilize the automated alignment system that is built into it. In order to use this feature, all the pieces must come together. The lamp intensity must be adequate, the etched image must have minimal distortion and the stepper job and reticle must be set up right.

From the data that was collected, it can be seen that the overlay error is repeatable. In the X direction, most of the measurements that were taken showed an overlay of + 2  $\mu\text{m}$ . All the measurements in the Y direction were 0  $\mu\text{m}$ . This says that the tool is capable of less than 1  $\mu\text{m}$  overlay error. In order to get the actual overlay capabilities of the tool, RIT needs a new overlay measurement system. With a box-in-box structure, the

overlay can be measured right on the Canon. It is possible to see less than 1  $\mu\text{m}$  overlay with a new vernier system as well. AVT has already created an overlay measurement system that can determine overlay error of less than 1  $\mu\text{m}$ . It is necessary for RIT to do this as well. As the RIT products become more advanced, the overlay tolerances will be more strict, just as it has for industry.

## 6. REFERENCES

- [1] James R. Sheats, Bruce W. Smith, *Microlithography: Science and Technology*, New York: Marcel Dekker, Inc., 1998
- [2] Alexander Starikov, Daniel J. Coleman, Patricia J. Larson, William A. Muth, "Accuracy of Overlay Measurements: Tool and Mark Asymmetry Effects," *Optical Engineering*, Vol. 31 No. 6, pp. 1298-1309, June 1992

## 7. ACKNOWLEDGEMENTS

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**Domenico DiPaola**, originally from Glasco, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2001. He attained co-op work experience at Eastman Kodak Company for 9 months and IBM for 6 months. He is joining IBM Corporation as an Engineer/Scientist in FEOL Lithography.



# Utilization of the Hitachi S-6780 SEM For Critical Dimension Measurement

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**Abstract** - The necessity of being able to accurately measure sub-micron features in devices fabricated in RIT's microelectronic manufacturing facility has resulted in the acquisition of a Hitachi S-6780 CD SEM. The Hitachi SEM will remove all user error, completely automate the current CD measurement procedure, and yield more accurate results. This project entails learning the operations of this model of SEM and the creation of various instruction manuals to allow this tool to become a commonly used piece of equipment at RIT. Explained will be the different kinds of files and measurement techniques the S-6780 SEM uses. Various experiments were performed and will be discussed proving the reliability and accuracy of this tool with measurement capabilities at RIT down to 0.3  $\mu\text{m}$ .

## 1. INTRODUCTION

As device critical dimension continues to rapidly decrease every year, improved methods of measurement need to be utilized. Presently RIT lacks a truly reliable method to measure our microelectronic facility's control over CD (critical dimension) size. To assist RIT in it's measurement capabilities a Hitachi S-6780 CD SEM (Scanning Electron Microscope) was acquired. Upon this tool's complete installation it has remained idle with only a select few individuals utilizing it. This small amount of usage is a direct result of time restraints of both professors and students and an overall lack of CD SEM operation knowledge.

To allow this tool to become a commonly used piece of equipment an operation manual was initially created. This manual will provide both students and faculty with instructions to run this tool. All basic commands along with many medium and some advanced operations were included.

Upon completion of the operation manual three experiments were performed with the Hitachi SEM. Each test measured a different set and size of five identical features arranged next to each other. The purpose of such experimentation was to prove the reliability and repeatability of the tool.

## 2. CREATION OF THE OPERATION MANUAL

To allow every person the ability to use the Hitachi S-6780 CD SEM a very descriptive operation manual was created. Included were twenty pages of a complete listing of all basic instructions along with many other advanced procedures. Three areas were focused on most heavily. These were the two files necessary for any measurement program to operate, the IDW (Identification of Wafer) and IDP (Identification of Position) files along with an automation program that incorporates these two files, the CP (Cataloged Procedure) file. Both instructions on how to create and run these files were included.

Displayed below in figure 1 is a complete listing of what is covered in the operation manual, shown is the operation manual's table of contents.

	Page Number
Turning on the SEM.....	1
Loading the measurement files (IDW and IDP).....	1
Flashing the tip.....	1
Loading the wafer.....	2
Beam adjustment and Focusing.....	2
Wafer alignment.....	4
Locating inspection points (manual).....	4
Locating inspection points (automatic).....	5
Manual CD measurements.....	5
Automatic CD measurements.....	6
Unloading the wafer.....	6
IDW file creation.....	7
IDP file creation.....	10
CP file creation.....	12
Running a CP file.....	16

Figure 1: Table of Contents of the Operation Manual

## 3. MEASUREMENT TECHNIQUE

RIT's present method of measurement utilizes two different scanning electron microscopes and an outside measurement program called Vital-Scan. This is a rather poor system allowing for much user error and is seldom

repeatable. Unlike this current method the Hitachi S-6780 CD SEM needs no outside assistance in measuring the critical dimensions of selected features.

### *Vital-Scan*

The Vital-Scan system is a high performance PC that is interfaced to the scanning electron microscope. This system allows the user to manually measure a line by clicking on the two edges of the feature, which is shown on the PC's monitor. According to where the user clicks, Vital-Scan will make the corresponding CD measurement. The largest problem with this system is all measurements are completely left to the user's ability to determine where the feature edge begins and ends.

Shown below in figure 2, a single resist line is measured by two different users with the Vital-Scan system. As can be seen, each user chose a different location for the beginning and the end of the feature edge, therefore resulting in two different CD measurements for on single line.

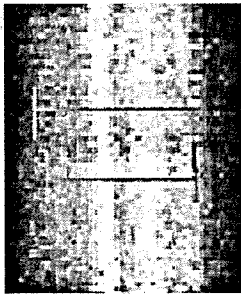


Figure 2: Resist line measured using Vital-Scan

### *Hitachi S-6780 CD SEM*

Unlike Vital-Scan the Hitachi CD SEM needs no outside assistance to measure CD sizes. The SEM has a built in program capable of determining the location of feature edges using one of two different methods: linear approximation or threshold.

With linear approximation the base and slope lines are linearly approximated and the intersection of the linearized line is used as a measurement point. A schematic of this is shown in figure 3

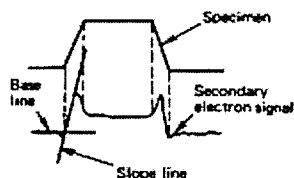


Figure 3: Linear Approximation

The second possible method, threshold, is used for examples where the feature edge is small, where the feature has good contrast. For the threshold technique the maximum and minimum signal intensities around the edges are determined and a threshold level is set up between them. The intersection of the threshold level and signal waveform is used as a measurement point. A schematic of this technique is shown in figure 4.

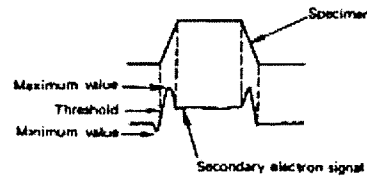


Figure 4: The threshold technique

## 4. EXPERIMENT

Once the operation manual was created three experiments were performed to prove the reliability and repeatability of the SEM. Three different CP files were created. This type of file stores a series of operational commands that the SEM automatically will carry out for the user.

The same wafer was used for each experiment. The wafer was coated with positive OIR 620 resist. A XLX 20 TARC (top anti reflective coating) layer was applied to the top of the resist. The wafer was then exposed using a Canon I-1 stepper, I line exposure. The Canon test reticle was used to pattern the wafer.

Each CP file would automatically align the wafer and then move to the measurement point, which was a set of five resist bars aligned in parallel next to each other. The set of five resist bars should have theoretically been identical in width and length. A drawing of the resist bars is shown in figure 5.



Figure 5: Drawing of resist bars.

The CP file would then increase magnification as to achieve a better image. It would then measure the width of each line at the exact same position. Each CP file measured a different size set of CD bars. The first experiment measured 1.0  $\mu\text{m}$  lines, the second experiment

measured 0.5  $\mu\text{m}$  lines, and the third experiment measured 0.3  $\mu\text{m}$  lines. For the final step of the experiment the SEM would calculate the following statistics for each set of five measurements: maximum, minimum, mean, and standard deviation.

## 5. ANALYSIS

Each experiment and appropriate CP file functioned correctly. In each experiment the appropriate lines were measured at the appropriate locations. The following six figures show the results of each experiment along with a SEM image of where the measurements took place.

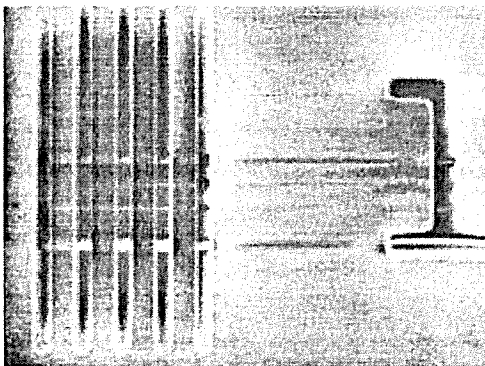


Figure 6: 1.0  $\mu\text{m}$  lines, magnified 20,000x

```
***** Measure Data *****
1. DATE       : 01-05-02
2. IDP FILE    : RESOLUTION-1
6. COMMENT     : 1 UM LINES
8. VACC (KV)   : 1.00
CHIP= (9, 0), MP= 1 DATA = 0.977
CHIP= (9, 0), MP= 2 DATA = 0.976
CHIP= (9, 0), MP= 3 DATA = 1.013
CHIP= (9, 0), MP= 4 DATA = 1.016
CHIP= (9, 0), MP= 5 DATA = 1.009

MAXIMUM      = 1.016
MINIMUM      = 0.976
MEAN         = 0.998
STDEV        = 0.016
```

Figure 7: Measurement data for experiment #1

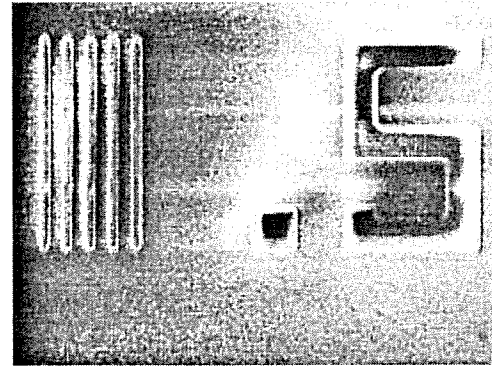


Figure 8: 0.5  $\mu\text{m}$  lines, magnified 20,000x

```
***** Measure Data *****
1. DATE       : 01-05-02
2. IDP FILE    : RESOLUTION-1
6. COMMENT     : 0.5 UM LINES
8. VACC (KV)   : 1.00
CHIP= (9, 0), MP= 1 DATA = 0.486
CHIP= (9, 0), MP= 2 DATA = 0.509
CHIP= (9, 0), MP= 3 DATA = 0.503
CHIP= (9, 0), MP= 4 DATA = 0.524
CHIP= (9, 0), MP= 5 DATA = 0.492

MAXIMUM      = 0.524
MINIMUM      = 0.486
MEAN         = 0.506
STDEV        = 0.015
```

Figure 9: Measurement data for experiment #2

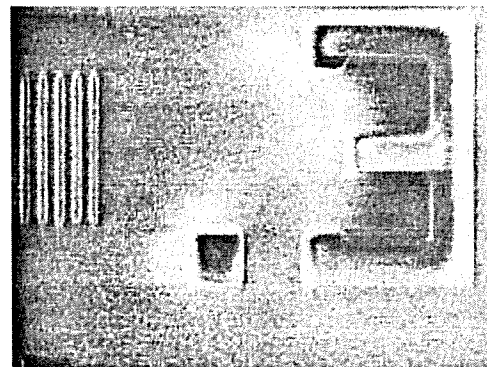


Figure 10: 0.3  $\mu\text{m}$  lines, magnified 50,000x

```

***** Measure Data *****
1. DATE       : 01-05-02
2. IDP FILE   : RESOLUTION-1
6. COMMENT    : 0.3 UM LINES
8. VACC (KV)  : 1.00

CHIP= ( 5, 4 ), MP= 1  DATA = 0.309
CHIP= ( 5, 4 ), MP= 2  DATA = 0.325
CHIP= ( 5, 4 ), MP= 3  DATA = 0.321
CHIP= ( 5, 4 ), MP= 4  DATA = 0.319
CHIP= ( 5, 4 ), MP= 5  DATA = 0.312

MAXIMUM      = 0.325
MINIMUM      = 0.309
MEAN         = 0.319
STDEV        = 0.007

```

Figure 11: Measurement data for experiment #2

## 6. RESULTS

The statistics of each experiments results are displayed in chart 1.

Feature Size	Mean	Standard Deviation
0.3 um	0.319 um	0.007
0.5 um	0.506 um	0.015
1.0 um	0.998 um	0.016

Chart 1: Experimental results

The mean feature width of each set of five resist lines was close to their optimum value. All standard deviation calculations were relatively small remaining below .016.

Experimentally through the completion of this project RIT now has the capability to accurately measure sub-micron CDs, the reliability and accuracy of the Hitachi CD SEM has been proven over a range of feature sizes, and an easily comprehensible set of operation instructions has been created.

## 7. CONCLUSION

This project involved the reliability and repeatability testing of the Hitachi S-6780 CD SEM along with creating a comprehensible set of operation instructions. Through three different experiments the SEM has proven to be a viable tool and can now be utilized by anyone in the microelectronics' facility.

## 8. ACKNOWLEDGEMENTS

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**Tim Footer**, originally from Palmyra, NY, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2001. He attained co-op work experience at VLSI

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# Optical Emission Spectroscopy for Plasma Etch Endpoint Detection

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**Abstract-** Optical Emission Spectroscopy was implemented for determining the endpoint of film removal through detecting shifts in plasma emission intensity during an etch process. A preliminary procedure has been developed for detecting endpoint with the factory nitride and oxide etch processes at RIT. In conjunction with the development of an endpoint process, the minimum sensitivity for the OES endpoint system was investigated. A minimum of 0.5% exposed nitride versus resist area is required for accurately detecting endpoint on Nitride, while 5% open area is necessary for Oxide.

## 1. INTRODUCTION

Through real time recording of plasma intensity over the full spectrum of optical emission, slight shifts in reacted chemistry can be detected [1]. Singling out specific peaks can indicate the completed etch through a desired film [2]. OES endpoint involves analysis of the light spectrum emitted from a plasma during an etch process. Plasma reactions result in discrete emission peaks dependent on the reactant chemistry in the chamber. Isolating emission peaks and recording the intensity over time allows for detection of a change of state in the process chamber. This change of state corresponds to the completion of an etch process.

Typical OES systems involve two main components, a CCD array for recording emission intensity and a computer system for recording the data and computing an endpoint signal. A fiber optic probe is used to gather light at the window of a plasma chamber, and transmit that light to a CCD array calibrated to record light intensity over the full spectrum of optical emission. Data is acquired through specialized computer software that enables real time statistical analysis and feedback, and archival for statistical modeling.

The sensitivity of OES for EP detection relies on detecting changes in the etch chemistry. Finding the minimum sensitivity is crucial as every new generation of semiconductor design involves geometry shrinks [7],[8]. As the geometry shrinks, the total amount of open area on

a wafer is reduced, and thus the amount of reactant chemistry in the plasma etch chamber is reduced. EP signals rely on separating the reactant chemistry from background noise for determining when the etch is completed. Current systems are detecting shifts on the order of 2% of the background signal. A portion of this experiment will involve determining if there is a limit to OES sensitivity. By varying the amount of open area on a wafer from a full 100% exposed film down to 0.1% open area, the sensitivity of OES will be investigated. Data will be collected based on a fixed etch time for purpose of analysis. Based on the recorded data, a best-fit model will be generated for determining EP. This model will then be tested, and successful EP detection will be determined through verification of etch completion.

Material requirements for the experiment were limited to available equipment. The challenge is to implement an endpoint system at RIT using the available tools consisting of an OES probe capable of detecting wavelengths between 200-1050 nm, and software from Ocean Optics for data acquisition. The computer system was a basic PC running Windows operating system, with an 800 mhz processor.

## 2. SUMMARY OF PROJECT OBJECTIVES

### *A. Implement plasma etch endpoint at RIT*

Available equipment was utilized to implement a data acquisition system for detecting endpoint during a plasma etch process.

### *B. Develop operating procedure for using OES system*

In order for the system to be utilized beyond this project, an operating procedure must be developed. This will include determining the simplest approach for implementing endpoint detection using real time OES measurements and developing a user manual for future operation.

### *C. Investigate OES sensitivity*

Determine the minimum amount of etch area that can be exposed, and still detect endpoint. This will be accomplished by varying the percentage of exposed film that is to be etched.

#### *D. Develop statistical model for analyzing endpoint signal*

The final goal of the project is to develop a new model for endpoint detection. Current endpoint processes involve complex statistical models for sorting through the enormous amount of recorded data to determine endpoint. For use at RIT, the simplest functional model would be ideal.

### 3. OES SETUP

The basic OES system is comprised of three main components. First is the computer, which is a basic PC that is fast enough to calculate and store the enormous amount of data generated by the OES systems. The heart of the OES system is comprised of a fiber optic probe for transferring the optical signal to the CCD array, which measures the emission intensity. An Ocean Optics OES system was used with a spectral sensitivity from 190nm to 1050 nm. The final component of the OES system is the software itself. Ocean Optics OOIBase32 program was used for data acquisition. Once data was recorded, it was transferred to Excel for analysis.

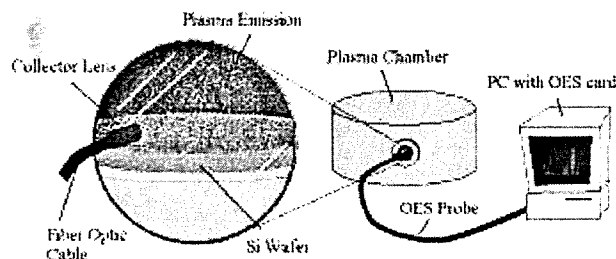


Fig.1. Diagram of OES process elements

The process for acquiring an emission spectrum as was done in this experiment is illustrated in figure 1. A fiber optic probe was temporarily mounted at the viewing window on the side of the plasma chamber. The probe was positioned to record emission near the center of the chamber, about an inch above the wafer. A collector lens at the end of the probe helped to boost the strength of the signal, as well as to average the emission signal for better data consistency. The gathered light is then sent to the CCD array via the fiber optic probe, which then measures the relative light intensity over the full spectrum of optical emission in fraction of nanometer increments. The software then sums the intensity data over a user defined

time interval. The integrated data is available for real time viewing over the full spectrum. Details of the data acquisition options for the OOIBase32 software package are available in the operating manual for the system.

After initial test measurements were made with the system, it was evident that the wavelength measurements were not accurate. The systems data acquisition was checked with the Ocean Optics Hg-1, mercury lamp emission calibration sample. It was discovered that the system had been improperly calibrated. The problem was that the software records data as pixel information and then applies a linear regression to label the wavelength axis on the plot. Changing the spectrometer channel settings back to the factory default calibration corrected the issue. Rechecking the Mercury sample indicated the wavelength was accurately displayed within  $\pm 0.1$  nm accuracy.

### 4. SENSITIVITY INVESTIGATION

Endpoint detection simply involves the detection of shifts in plasma emission intensity over time. Plasma emission is however a complex function of the reaction between etchant species and the film to be etched. In addition there is emission from uncontrolled processes in the chamber such as the resist on the wafer. As less film is exposed to the chamber versus the amount of resist covering the wafer, the signal to noise ratio is greatly reduced. The minimum sensitivity for EP detection can then be described by the smallest percentage of the wafer with exposed film to be etched versus resist that yields a detectable EP signal.

#### *A. Preparation*

Before the experiment could begin, a process had to be developed for creating a resist pattern with an exact percentage of open area. The goal was to develop a resist coat, expose, and develop process for creating open areas on the wafer totaling 5%, 1%, 0.5%, and 0.1%. First the actual dimensions of the wafer were measured to determine the total wafer surface area. The total wafer surface area was calculated to be  $77.82 \text{ cm}^2$ , or  $7.78\text{E}9 \text{ } \mu\text{m}^2$ .

The next step was to pick an existing mask to use. The CMOS test mask via and metal2 layers were chosen due to the uniformity of features present on the mask. The features on the mask were equal sized squares with similar spacing between features. The total open area generated at the wafer surface was calculated as  $716,000 \text{ } \mu\text{m}^2$  for the via mask and  $846,000 \text{ } \mu\text{m}^2$  for the metal2 mask. Using these numbers, the total amount of repeated exposures necessary to generate the desired percentage open area was calculated as follows.

% Open Area	Mask	# Repeated Exp
0.10%	Via	11
0.50%	Metal 2	46
1%	Metal 2	92
5%	Open	13

Table 1. Mask used for percent area

Once the desired film was deposited on each wafer, the standard RIT resist process was used for patterning. Wafers were coated with positive resist using the 4" Wafertac. A program had to be written for exposing each desired percent open area using the GCA g-line stepper. Once exposed, wafers were developed using the standard process and then each wafer was carefully inspected for accurate pattern generation and desired film thickness. Wafers at this point were ready for the etch experiment.

### B. Oxide Etch Experiment

Preparation for the oxide etch involved growing a thermal SiO<sub>2</sub> layer, and patterning the wafers with the appropriate percent open area. 18 cleaned wafers labeled EP-01 thru EP-18 were loaded into the automated oxide furnace, using recipe 350 for 5000Å of oxide growth. Following is a plot of the resulting oxide thickness for each wafer.

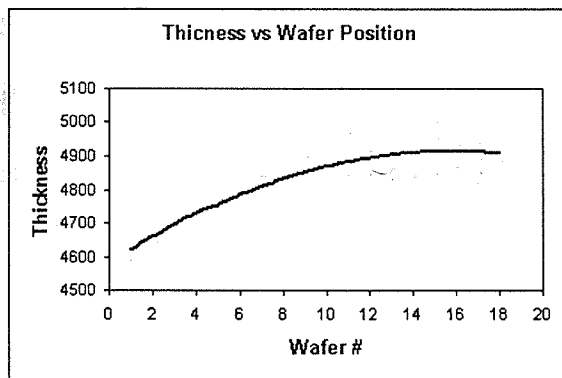


Fig. 2. Oxide thickness variation by wafer

Next, resist was deposited and patterned for each wafer with the following open area parameters.

Wafer #	% Open Area
1-3, 18	0.10%
4-6	0.50%
7-9, 17	1%
10-12, 16	5%
13-15	100%

Table 2. Percent open area by wafer

Before running an experimental wafer, a blanket resist test wafer was run to determine the effectiveness of the OES system for detecting an EP signal. The default resist etch recipe was used with no modifications. Data acquisition was set to integrate over 500 msec intervals with a 50 msec delay. Observing the full spectrum 4 min 19 sec into the etch, there were 4 major peaks that dropped significantly. The etch was manually stopped and the wafer was analyzed for residual resist. With the wafer cleared, it was determined that EP was detected for the resist process.

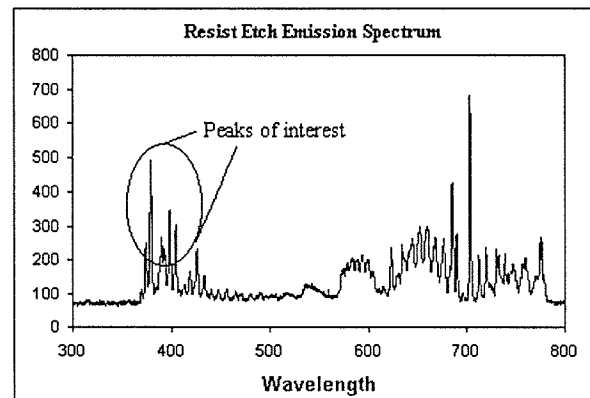


Fig. 3. Resist sample emission spectrum

Chamber 3 on the DryTek Quad RIE etch tool was used for the oxide etch. Prior to running the etch, the chamber was seasoned for 10 minutes. Seasoning the DryTek involves running the chamber in the chemistry to be used for the etch process in order to purge the chamber and gas lines of any impurities. The OES system was run during the seasoning to acquire data for the emission of the etch chemistry alone. The main etch parameters for the factory oxide etch are as follows.

Chemistry: 30 sccm CF<sub>4</sub>, 60 sccm CHF<sub>3</sub>, 60 sccm Ar  
 Pressure: 200 mT  
 Power: 300 watts

The initial power was only 100 watts yielding an etch rate of only 200Å/min. Increasing the power to 300 watts achieved an etch rate of about 550Å/min.

The final preparation before running the experiment was to determine the effectiveness of the etch process for the varied experimental parameters. The etch rate of the resist in the oxide etch chemistry was determined to be 200

A/min. This was checked to be sure that the increased power did not cause the resist to be removed completely during the etch. After correcting calibration issues that arose during the preliminary work, and adding a larger hard drive to the OES computer to account for the massive data files being generated, it was time for the full processing run.

Preliminary etch work with test wafers EP-16 and EP-17 demonstrated that the smaller open area wafers required a longer etch to fully clear the oxide film. This was an interesting effect, considering the wafers with smaller percent open areas also had a thinner oxide film from deposition. The etch time was compensated accordingly and all wafers were run sequentially in the etch chamber.

Wafer	Open Area	Etch Time
13-15	100%	10 min
10-12	5%	12 min
7-9	1%	12 min
4-6	0.5%	12:50 min
1-3	0.1%	13:20 min

Table 3

During the etch process, there were four major peaks from 400 nm to 500 nm that were most noticeably affected by the change in open area. Upon completion of data acquisition, a CD was burned with all information for later analysis.

### C. Nitride Etch Experiment

After completion of the oxide etch process, all wafers were stripped of resist. The remaining oxide film was removed in buffered HF, and the bare Si wafers were cleaned using the RCA clean. With the cleaned wafers, a pad oxide was grown prior to nitride deposition for the purpose of stress relief and as an etch stop layer. An average of 650Å of oxide was grown on each wafer using the Kooi recipe in the automated furnace.

Next was the deposition of nitride in the LPCVD furnace. The RIT standard 2.5:1 nitride recipe was used with a deposition rate of approximately 40 Å/min. Following deposition the nitride thickness was measured across every wafer. The resulting thickness was an average of 1000Å of nitride with good wafer-to-wafer uniformity.

Once measured, the wafers were prepared with the appropriate open area, using the same procedure as the oxide etch experiment. After development, all wafers were checked and prepared for the etch process.

The factory nitride etch recipe was verified prior to running the experiment. The following etch parameters were used.

Chemistry: SF<sub>6</sub>  
Pressure: 300 mT

Power: 280 watts

The etch rate of nitride was tested for a blanket film and was determined to be 660 Å/min. Checking the etch rate of the smaller percentage open area verified that the etch rate was slower, therefore the etch time was compensated for each subsequent level of open area. The etch times that were chosen are shown in table 4.

Wafer	Open Area	Etch Time
13-15	100%	2:20 min
10-12	5%	2:30 min
7-9	1%	2:30 min
4-6	0.5%	2:45 min
1-3	0.1%	2:45 min

Table 4

After verifying that the etch parameters would work for all experimental settings, the process was started. The etch was run in chamber 2 of the DryTek Quad. Prior to beginning the experimental wafers, the chamber was seasoned with the nitride etch chemistry for the required ten minutes. Data was recording with the OES system for comparison of the raw etch chemistry with the actual etch run data. All wafers were sequentially etched with the data being archived to a CD upon completion of the experiment.

## 5. DATA ANALYSIS

Gathering all of the experimental data illustrated one of the complications associated with using OES for EP detection. The total amount of data recorded from etching 36 wafers combined with all the preliminary data exceeded 2 GB. To make matters worse, the Ocean Optics software package stores the data in individual text files for each time interval. For the oxide data, this exceeds 1300 text files per wafer etched. In order to analyze the data, there was a definite need to compress the information into a single file.

### A. Extracting the data

Using Excel, a macro was written for extracting the data from the individual text files and importing them into a single Excel workbook. All text files for a single wafer run were placed in a temporary folder. From here each text file is opened and the emission intensity data is cut and pasted into a single workbook. Each column in the new workbook contains the emission data for a specific time increment. After writing and debugging the macro, all of the data was sorted and extracted into separate Excel files for each wafer run. The extracted data was then archived to 5 zip disks and analysis could begin.

### B. Determining a basic EP model



From previous experience with industrial EP systems, the simplest model was chosen and implemented to verify the data. First, two peaks are chosen to ratio over the full etch time. The goal is to find a ratio of peaks that yields a consistent wafer-to-wafer signal indicating EP. It is important to note that when looking at the peaks, the data is given in fraction of a nm increments. Singling out a single fraction may result in poor results, as there are many slight variations in the signal over time and across wafers. Instead a band pass of 30 data points is summed in order to get a more consistent signal. In essence the data is integrated over a short interval to enhance the uniformity of the EP signal.

Choosing individual wavelengths is a combination of known chemistry and visible changes in the spectrum. Observing data collected during the etch process, significant peaks can be pinpointed. The nitride etch data was the first set looked at due to the relatively simpler emission profile.

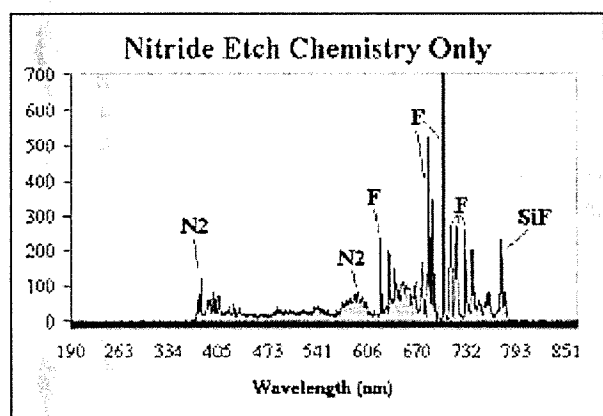


Fig. 4. Spectral emission during nitride seasoning

Figure 4 illustrates the basic nitride etch chemistry while seasoning the chamber. The wafer with blanket nitride was then compared with the data for seasoning the chamber.

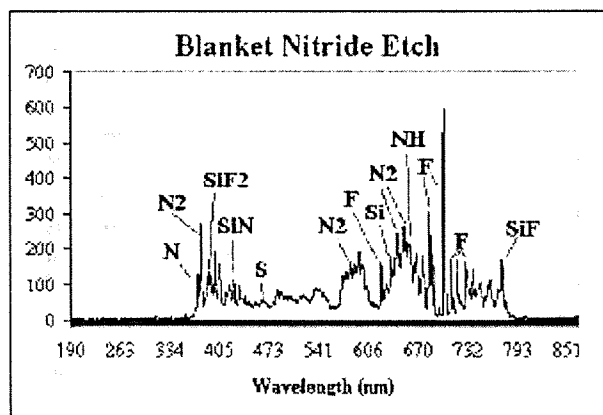


Fig. 5. Spectral emission during nitride etch

Observing the significant differences between the blanket nitride etch and the seasoning data, a few areas of interest were looked at in detail. Segregating these portions of the data out, peaks were compared during the full length of the etch process to determine which peaks showed the most significant variation, indicating EP. Analysis demonstrated the most significant ratio between the N<sub>2</sub> peak at 385 nm versus the fluorine peak at 685 nm.

The process was repeated for the oxide data.

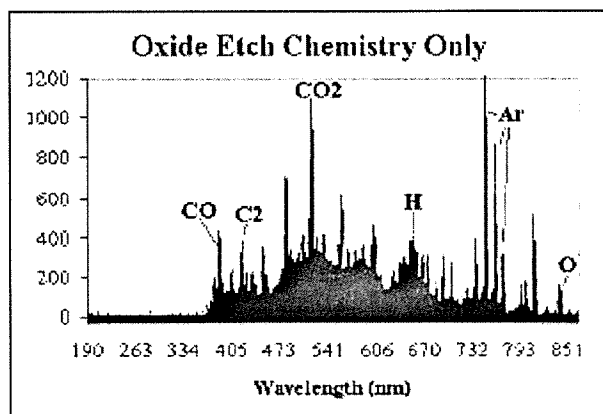


Fig. 6. Spectral emission during oxide seasoning

The oxide seasoning data shown in figure 6 illustrates the complexity of the emission profile relative to the nitride data.

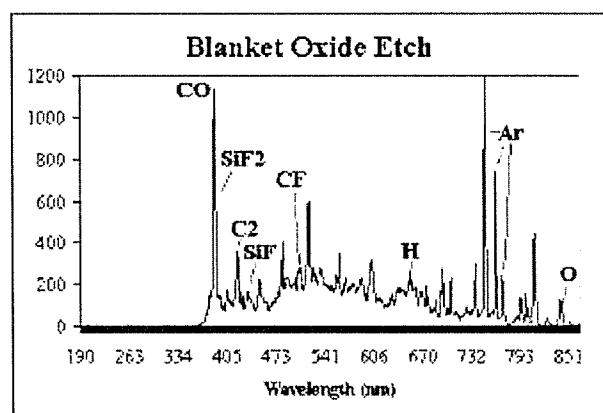


Fig. 7. Spectral emission during oxide etch

Comparing the seasoning data with the blanket oxide etch data demonstrates a significant difference at 380 nm. The peak at this location is a combination of CO and SiF<sub>2</sub> emissions. Examining all the data was complicated by the amount of noise that was present in the signal. The best results that were obtainable were with a ratio of the CO peak at 380 nm with an argon peak at 750 nm.

## 6. RESULTS

The major accomplishment was successful implementation of endpoint detection at RIT. The result is a functioning OES system for post processing endpoint detection. The available software package has the capability of displaying peak ratios in real time, however, true real time endpoint detection will require additional software. In addition a series of Excel macros were written for analyzing the precise time of etch completion, which will allow feedback for etch rate, and amount of over etch. Use of the system will provide students with a valuable introduction to endpoint detection as used in industry today.

Results for the sensitivity investigation were obtained through use of the peak ratios that were determined in the full analysis of the data. EP traces were then plotted for each wafer in the investigation and were comprised of only the ratio between peaks. For determining the actual EP time, the slope of the plot was analyzed versus time in order to generate a more sensitive model. The time was chosen as the point where the rate of change in the slope was reduced to a set value.

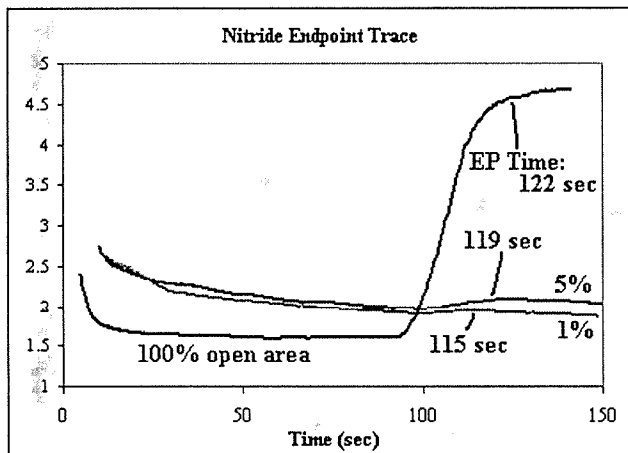


Fig. 8. Nitride EP trace for 100% to 1% open area

Figure 8 illustrates the incredible signal that was generated by the full nitride wafer reaching endpoint. Further analysis of the data provides insight into details of the process chamber, including etch uniformity.

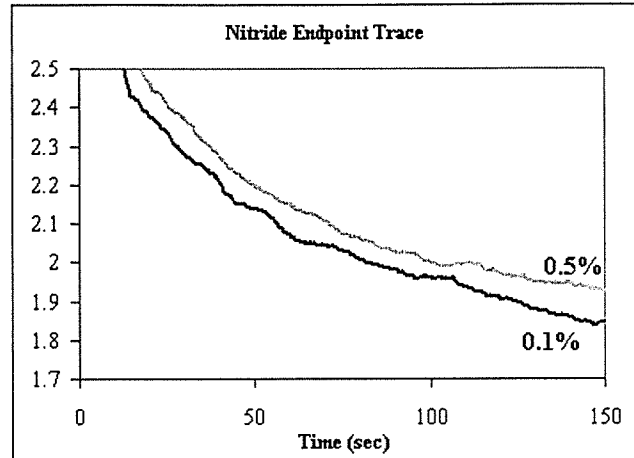


Fig. 9. Nitride EP trace for 0.5% and 0.1% open area

Comparing the EP signals in figure 8 with those of the 0.5% and 0.1% open area wafers demonstrates the diminished sensitivity of the OES system as the open area is reduced. The height of the EP transition is directly related to the amount of open area. From this knowledge, the minimum sensitivity can be determined if the level of background noise is known. A minimum signal to noise ratio of 2:1 is recommended for consistent EP detection.

The oxide etch signal had a much greater amount of background noise. The result was an EP trace as follows in figure 10.

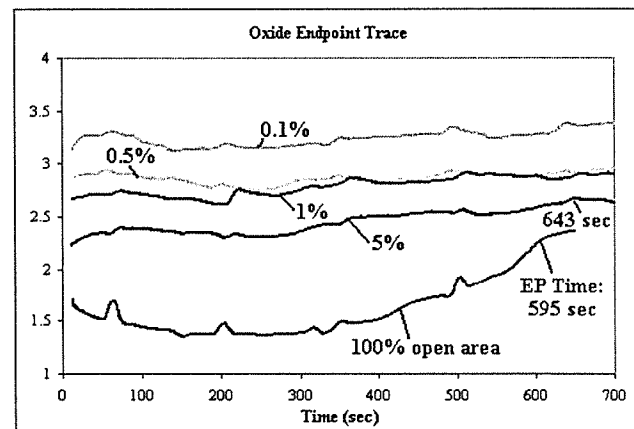


Fig. 10. Oxide EP trace for 100% to 0.1% open area

Analyzing the trace indicated an accurate signal with a minimum of 5% open area. The complexity of the etch chemistry contributed to the degradation of the signal. It is also possible that what was detected as noise could have been due to a fault in one of the gas lines that feeds the oxide etch chemistry, or in the plasma chamber itself. However, constraints surrounding this experiment eliminated the option of investigating these possibilities. Further analysis of the oxide data could indicate a better set of peak ratios.

## 7. CONCLUSION

Post processing etch endpoint has been successfully implemented at RIT. In addition, experimental data illustrated the difficulty in detecting EP with small amounts of open area on the wafer. Nitride etch endpoint has been demonstrated with a maximum sensitivity of 0.5% exposed nitride. Oxide endpoint capabilities have so far been proven down to 5% open area. Real time EP detection is possible with the current setup through careful manual operation of the OES system. Automated EP will only be possible with the addition of new OES software and system upgrades to the plasma etch chamber.

## REFERENCES

- [1] H. H. Yue, S. J. Qin, R. J. Markle, C. Nauert, M. Gatto, "Fault Detection of Plasma Etchers Using Optical Emission Spectra," IEEE Trans. on Semicond. Manuf., Vol. 13, No. 3, Aug 2000, pp. 347-384.
- [2] D. A. White, B. E. Goodlin, A. E. Gower, D. S. Boning, H. Chen, H. H. Sawin, T. J. Dalton, "Low Open-Area Endpoint Detection using a PCA-Based T/sup 2/ Statistic and Q Statistic on Optical Emission Spectroscopy Measurements," IEEE Trans. on Semicond. Manuf., Vol. 13, No. 2, May 2000, pp. 193-207.
- [3] R. M. de Castro, P. Verdonick, et al, "End-Point Detection of Polymer Etching Using Langmuir Probes," IEEE Trans. on Plasma Sci., Vol. 28, No. 3, June 2000.
- [4] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*. New York: Wiley, 1994.
- [5] C. Riccardi, R. Barni, F. De Colle, M. Fontanesi, "Modeling and Diagnostic of an SF<sub>6</sub> RF Plasma at Low Pressure," IEEE Trans. on Plasma Sci., Vol. 28, No. 1, Feb. 2000, pp. 278-287.
- [6] K. Nanbu, "Probability Theory of Electron-Molecule, Ion-Molecule, Molecule-Molecule, and Coulomb Collisions for Particle Modeling of Materials Processing Plasmas and Gases," IEEE Trans. on Plasma Sci., Vol. 28, No 3, June 2000, pp. 971-990.
- [7] International SEMATECH, "Unified Equipment Performance Metrics for 0.18 um Technology," Technology Transfer # 99093826A-TR, November 19, 1999.
- [8] International SEMATECH, "Unified Equipment Performance Metrics for 130 nm Technology, Version

2.0," Technology Transfer # 99123857B-ENG, July 10, 2000.

- [9] C. J. Spanos, K. Poolla, "Modeling and Controlling Variability in the Intelligent Factory," Final Report, 1995-96, Micro Project #96-022.
- [10] P. Simon, J. M. Luchies, W. Maly, "Identification of Plasma-Induced Damage Conditions in VLSI Designs," IEEE Trans. on Semicond. Manuf., Vol. 13, No. 2, May 2000, pp. 136-143.
- [11] N. Layadi, T. Lill, J. Trevor, S. J. Molloy, F. Baumann, M. N. Grimbergen, T. C. Esry, J. Chinn, "Interferometry for Endpoint Prediction in Gate Etching," Adv. Semicond. Manufac. Conf. and Workshop, 1999 IEEE/SEMI, 1999, pp. 227-232.

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**Keith R. Miller** was born in small town north of Los Angels, California January 11, 1977. At the end of this paragraph, he will have completed his Bachelor of Science degree in Microelectronic Engineering from RIT. His career will be starting with Advanced Micro Devices in Sunnyvale, California, working as a rotational engineer in the Submicron Development Center.

# Cross Sectional Analysis of IC Devices Using Polishing Techniques and SEM Imaging

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**Abstract--** The purpose of the project was to develop a universal procedure for obtaining a cross section of various IC devices, use a Scanning Electron Microscope (SEM) to document these devices, and identify different layers and try to obtain dimensions for the devices. The technique was developed using a mechanical polishing procedure followed by a chemical mechanical polishing step, and worked as expected, producing very good images of the cross section of various film stacks and devices. Wide ranges of devices were analyzed to test the robustness of the process. Film stacks could be measured in both thickness and composition (with the proper equipment), and very clear high magnification images of devices were obtained.

## 1. GOALS

The main goal of the project was to develop a universal procedure for obtaining a cross section of various IC devices at RIT. Secondary to this, the cross-sectioned devices were then to be imaged using a Scanning Electron Microscope (SEM) and compositional and dimensional information were then to be obtained.

## 2. BACKGROUND

The need for a process to obtain good cross-sectioned images at RIT is apparent in that all of the equipment to make and test IC devices is present, but a method of looking at the internal structure was not. The only method used previously was that of scribing and cleaving, which is not accurate and is problematic when there are multiple films present. Therefore, based on previous work at Dominion Semiconductor (a wholly owned subsidiary of Toshiba manufacturing DRAM and Flash memory) in the Failure Analysis laboratory, the tripod polishing method used there was decided on. This decision was made based on the availability of the equipment and relatively low expense (to RIT) of developing such a process. As previously work had been done in this area with Dominion

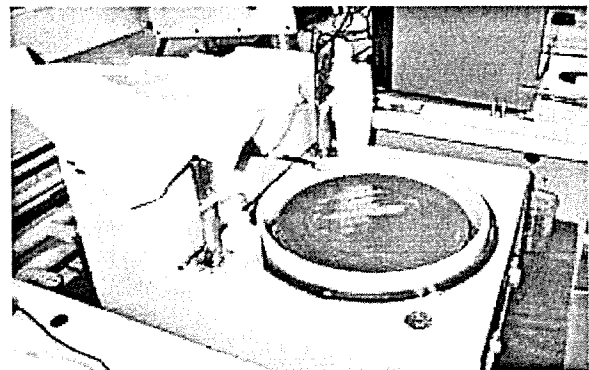
Semiconductor, an idea of the equipment and process was already in place.

## 3. EQUIPMENT

Various equipment was needed to accomplish the aforementioned goals. Some equipment was already available at RIT and some needed purchasing in order to provide a process. South Bay Technology, Inc. was contacted as they had a tripod polishing setup on the market that would suit RIT's needs.

### *A. Polishing Wheel*

The equipment and process outlined by South Bay Technology required a variable speed polishing wheel with a glass plate as the polishing surface for mounting lapping films. The wheel also required a water supply and drain as the polishing done was of a wet nature. A variable speed polishing wheel with water supply and drain was available at RIT and a compatible glass plate was ordered from



South Bay Technology. This was then custom mounted to the polishing station

Figure 1: Polishing wheel fitted with glass plate polishing surface.

## B. Lapping Films

A set of diamond impregnated lapping films compatible with the glass plate polishing surface was also obtained from South Bay Technology. These were in six different film sizes starting with 30 micron and going down to .5 micron. These will be discussed further when the process is outlined.

## C. Tripod Polisher

The samples to be cross-sectioned needed to be mounted in a tripod which would sit on the lapping films as the wheel rotated. This was also ordered from South Bay Technology and is outlined below.

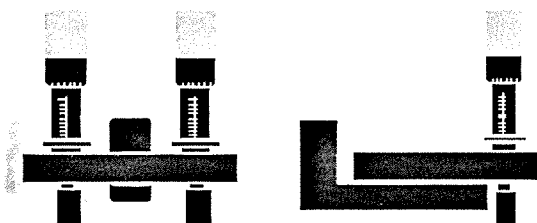


Figure 2: Figures obtained from South Bay Technology literature showing side and back views of the tripod. Sample mounts on the left most point facing down from the side view, and in the center facing down from the back view.

The tripod polisher has sample mounting such that the sample can be removed directly from the apparatus and placed in a SEM for examination. The back feet have integral micrometers for adjustment during polishing to ensure that the sample is polished coplanar to the target area.

## D. Microscope

A microscope is needed to adjust the sample in the tripod while polishing to ensure coplanarity with the target area. It is also used in sample mounting to get the sample roughly straight on the mounting stub. The microscope must have enough room to fit the complete tripod on end under the objective. This was available at RIT.

## E. Colloidal Silica and Compatible Polishing Pad

For the final polishing step (outlined in the procedure), a colloidal silica .05-micron slurry is needed along with a compatible polishing pad. This was present at RIT in the CMP department.

## F. Sample Mounting

SEM stubs that mount directly into the tripod polisher were part of the tripod package from South Bay Technology. Mounting the samples required a hotplate and polymer with high boiling point relative to its melting point (also supplied with the tripod kit) which was melted on the stub in preparation for the sample.

## 4. PROCESS

The process used to polish the samples was based on the recommendations of South Bay Technology and past experience at Dominion Semiconductor. Application of the process to the equipment available at RIT was done by experimenting with polishing speeds with the various lapping films to where a manageable and comfortable polishing rate was achieved without causing damage to the films or sample. This was done as a trial by error as it had more to do with equipment preferences than anything else.

First, the sample was mounted on the supplied SEM stub by placing the stub on a hotplate at 120 degrees Celsius. Some of the aforementioned polymer glue was then placed on the stub. A sample approximately one centimeter by 5 millimeters was then placed on the stub and positioned so that the target area was hanging off the edge of the stub by approximately 3 millimeters. The sample is then immediately placed under a microscope and, while the glue is still hot, straightened to the edge of the stub as best as possible. Once this is done, the stub is allowed to cool for a minute or two and then mounted in the tripod.

Once mounted in the tripod, the micrometers on the back feet of the tripod must be adjusted to the same height as the target area on the sample. This is to assure that the cross-section occurs at a right angle to the top surface of the sample.

Next, the first lapping film must be mounted on the polishing wheel. This is done by first wetting the glass wheel and then placing the film down on top of the glass. The water must then be pushed out from under the film by using a rubber or plastic spatula. The film will then stick to the wheel held by suction.

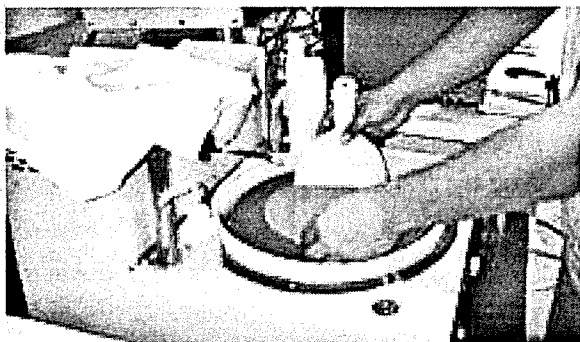


Figure 3: Mounting of the lapping film using wet adhesion.

The tripod is then placed on the rotating wheel back first. The sample end of the tripod is slowly placed in contact with the wheel and no pressure is applied. The only pressure is that to hold the tripod in place on the wheel. The tripod should be placed with the sample facing the direction of rotation.

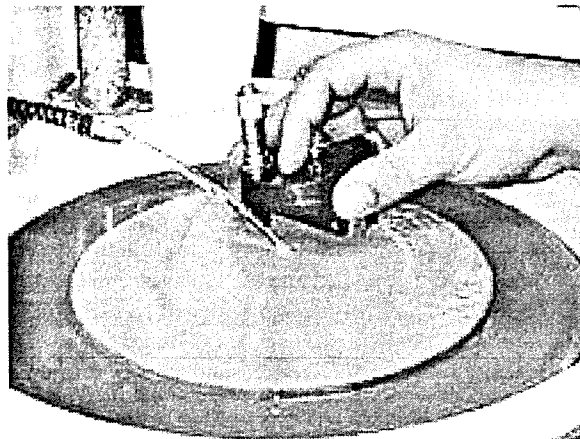


Figure 4: Bringing the sample into contact with the wheel.

A paper towel should be placed over the trail of polishing debris so that the sample is not scratched and the film does not get clogged or burnt.

The speed of the polishing wheel depends on the film used and also the operator. The polishing rate must be kept at a manageable level so that the target area is not overshot or undershot. Table 1 shows the procedure best able to control the polishing rate using the available equipment.

Table 1: Shows process obtained for given equipment.

Film	Speed	Comments
30 $\mu\text{m}$	130rpm	Uniform scratches on entire surface. Inspect under microscope and adjust micrometers parallel to plane of interest.
15 $\mu\text{m}$	100rpm	30 mm scratches completely removed. Polish until plane of interest is ~ 300 mm away. Inspect under microscope to ensure the polishing plane is parallel to the plane of interest.
6 $\mu\text{m}$	70rpm	15 mm scratches completely removed. Polish until plane of interest is ~ 100 mm away. Inspect under microscope to ensure the polishing plane is parallel to the plane of interest.
3 $\mu\text{m}$	50rpm	6 mm scratches completely removed. Polishing plane should be parallel to the plane of interest, make final adjustments.
1 $\mu\text{m}$	30rpm	3 mm scratches completely removed. Plane of polish should be parallel with the plane of interest.
.5 $\mu\text{m}$	15-20rpm	1 mm scratches completely removed. Polish until plane of polish is just outside the plane of interest. Inspect under inverted microscope to locate the area of interest.
.05 $\mu\text{m}$ Colloidal Silica	30rpm	Use Polishing cloth. Polish for 30 seconds to a minute in the opposite orientation. Clean immediately with Q-tips. Rinse cloth.

After the 30, 15, and 6 micron polishing steps, the sample needs to be examined under a microscope while still attached to the tripod to ensure the polishing is occurring co planar to the target area. If it is not, the micrometers need to be adjusted to straighten it. If an adjustment is needed, polish on the same film for ~5 seconds so as to not damage the next film. By the time the three micron polish is complete, adjustments should be finalized.

The final film (.5 micron) must be used very carefully as it is easily damaged and the target area can be overshot on the sample. Frequent examination and slow polishing speeds are important for this step.

The final polish is done using a .05 micron colloidal silica slurry on a compatible polishing cloth at 30 rpm. This is done in the opposite direction, with the sample facing away from the direction of rotation, and it's purpose is to remove all scratches left on the surface. It can be done for 30 seconds to one minute. The sample must then be cleaned, usually done by rinsing under water and rubbing with a q-tip that has some soap on it. This is to remove all of the remaining slurry on the sample. It is very important to completely clean the polishing pad when finished as if slurry dries on it, the sample will be scratched when it is used again. Also, the glass plate on the polishing wheel must be kept clean as any dirt on it can scratch the sample or damage the films placed on it.

## 5. RESULTS

Very high quality images were obtained using the above outlined process. The images taken were done on a LEO Scanning Electron Microscope. At high acceleration voltages, the images obtained were excellent.

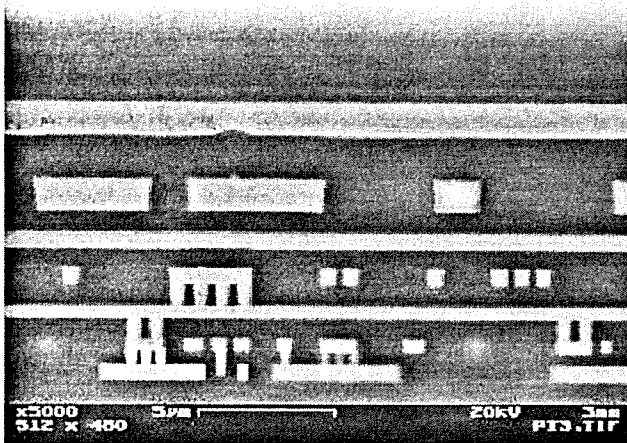


Figure 5: Image of industry chip taken at 20kV, 50000x magnification

The various layers were identifiable and had very good contrast. Scratches were not evident.

For the first round of samples prepared, the final polishing step was not performed as it was thought to be unnecessary. At lower acceleration voltages (~2kV), however, scratches became apparent. This made looking at thin film layers and grains of various layers very difficult. Once the final polishing step was performed, the

images were excellent, even at acceleration voltages as low as 1kV.

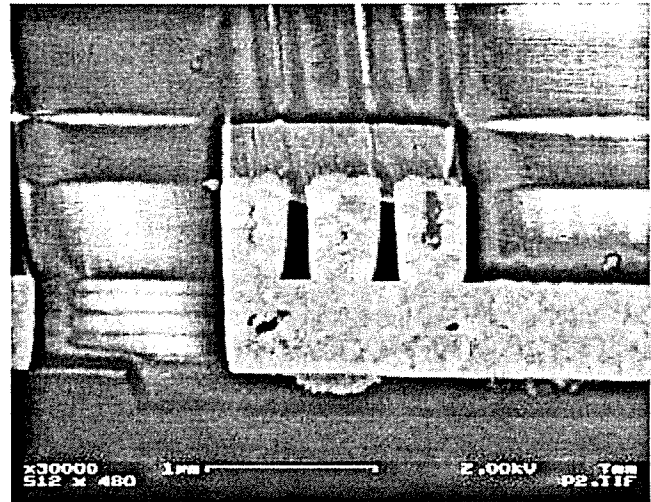


Figure 6: Image of Industry chip taken at 2kV, 80000x magnification. Notice the grain of the tungsten (lighter) layer.

Compositional information and various film thicknesses were also obtained using various methods (EDAX x-ray and computer aided measurements).

## 6. CONCLUSION

The polishing procedure developed for the equipment available at RIT was very successful, obtaining very high quality SEM images of various structures. This was done at a minimal cost as opposed to other methods, and was more successful than originally anticipated. All of the goals set forth were achieved and RIT is now more capable as a facility, especially in the failure and device analysis areas.

## ACKNOWLEDGMENTS

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# Incorporation of Control Charts into a Manufacturing Execution System

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**Abstract** – The wafer fabrication facility at RIT has a primary goal of being a teaching facility. Tracking of the student run wafer lots is accomplished very effectively by MESA, a lot-tracking software package. The system is configured to collect information, but database queries were not set up to display this information. MESA has the option of outputting information from the databases to a statistical software package called Quality Analyst. Quality Analyst displays control charts for the extracted data, providing quick, visual interpretation of the process in question. The adaptation of this software into the RIT Microelectronic Engineering fabrication facility has been achieved. Full realization of the impact on wafer yields has not been extracted so far, but insight into process improvement has already begun.

## 1. INTRODUCTION

Rochester Institute of Technology is home to the student run Microelectronic Engineering facility. The facility is capable of running both 4" and 6" CMOS processes, consisting of about 70 total process steps each. The information resulting from each of the steps is stored on a centralized computer database. RIT's software of choice is MESA by Camstar Systems Inc. MESA stands for Manufacturing Execution System Application and provides the necessary user interface and database connectivity for tracking the entire student processed lots.

This system has provided the means of collecting and storing the information since it was first installed. However, gathering the information in the form of a query was quite tedious and required certain access privileges. This meant that interpretation of the data was left to a few select users, generally after the runs had long since been completed. A system of control charts was needed to effectively manage the data being collected so improvements to the equipment running the lots could be made. In addition, preventive maintenance schedules could be altered to improve the amount of money RIT would have to spend on key components.

It was decided that Quality Analyst, a statistical software package from Northwest Analytical, would be incorporated into the current system to provide the aforementioned improvements [1]. Because RIT's facility is a

teaching one, further instruction beyond just displaying the control chart was deemed necessary for completeness. After investigating MESA's capabilities, the best method to get the interpretation information to the operators was through Microsoft PowerPoint. The combination of all of these elements would provide the means of collecting, displaying, and interpreting the information, real-time.

## 2. PROCEDURE

RIT's Microelectronic Engineering facility already owned the necessary hardware, software, and licensing to complete the project. Most of the required steps involved the programming and configuration of the software in use.

### A. MESA Setup

It was decided that the simplest approach to solving the problem of requiring instructions along with a graphical output of a chart was to let MESA interface directly to Microsoft PowerPoint first. This was accomplished right in the instructions for processing the lot. A user would enter a "1" in the column on the process instruction screen to display the associated document. (See figure 1) This document was previously created in PowerPoint and was a standalone show (\*.pps) that would automatically run.

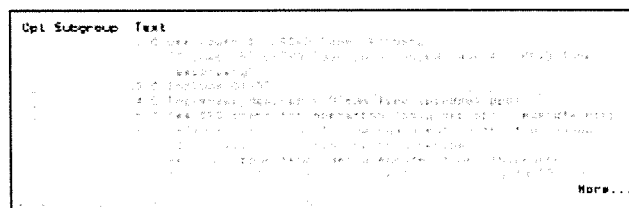


Figure 1 – Command to display SPC chart

The other, more important, setup required for MESA was the actual database queries themselves. A lot of information is stored with the lot data that is collected, such as time of day, operator name, etc. The desired information for displaying on the control charts needed to be sorted out and selected for automatic extraction. In addition, individual names to these queries were needed for later access not only in the MESA screen but also through the open database connectivity (ODBC) driver that Quality Analyst used [2].



### B. PowerPoint Setup

The simplest of all to setup were the PowerPoint shows. These were all based on a similar format, allowing the operators to become familiar with the universal layout quickly and easily. The first page gives a basic summary of the information about to be presented. (See figure 2) It displays links for the user to either display the current control charts, both an x-bar and a process capability chart, or an action plan to take when the control chart displayed is out-of-control. The action plan is simply another PowerPoint slide, whereas the link to the control charts is a Quality Analyst run file that causes Quality Analyst to start.

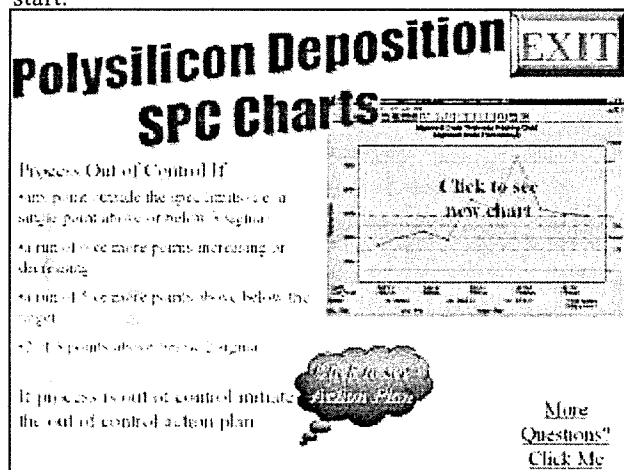


Figure 2 – PowerPoint instructions and chart link

### C. Quality Analyst Setup

The most complicated setup was that of Quality Analyst. This is because Quality Analyst creates both a header file (\*.hed) and a run file (\*.run). The header file defines the variables to display, the data range, control limits, and axes titles from the database query. The run file defines which query to run, where to temporarily store the data, and which charts to display.

Most of the time and effort put into setting up Quality Analyst comes in forming the header file. Thankfully, most of this was easily accomplished through a graphical user interface. The terms chosen for control chart investigation were the lot dates and the mean of the run (film thickness, critical dimension width, etc.). Once the terms were chosen for the charts, the run file needed to be created to read in the data. Using the "connect" command, this causes Quality Analyst to issue a command to MESA, making a brand new chart of the most up to date information. Lastly, the two charts that were initially integrated were the x-bar and process capability charts.

## 3. RESULTS

Microsoft PowerPoint and NWA Quality Analyst were successfully integrated with the current MESA setup. The CMOS p-well revision 3 process was the only one setup for control charts, but further integration could easily be accomplished. Results for a typical control chart display are shown in figure 3. It was chosen to display both the x-bar and process capability charts at the same time on the user's display, for correlation purposes.

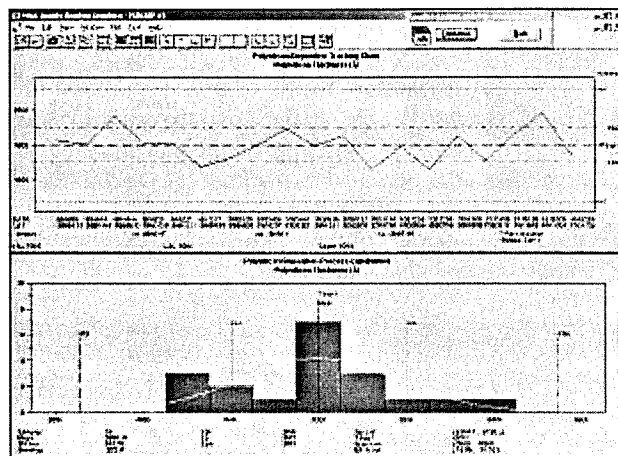


Figure 3 – Quality Analyst SPC charts

Automatic access of the database without an upper level access password is automatically configured when the user logs on to the MESA system. This allows for universal access to the data on the local intranet. In addition, when properly configured, any user could also connect to the system via the Internet.

Equipment results for process capability and preventive maintenance schedules have yet to be determined. The information gathering phase was set to begin upon the completion of this project.

## 4. CONCLUSION

Integration of the graphical means of analyzing the data collected by MESA was a key improvement to the wafer fabrication facility at RIT. A complete instruction set for creating the required control charts from step one was also created for further statistical integration into RIT's advanced CMOS processes. Further investigation into some of the preliminary process limits will come as the control charts help to improve the equipment in use.

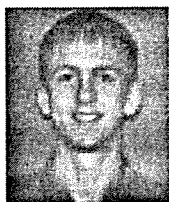
## REFERENCES

- [1] "NWA Quality Analyst User's Manual," Northwest Analytical Incorporated, 1999.

[2] "Statistical Process Control Reference Manual (Release 2.0), Camstar Systems Incorporated, 1999.

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# Dry Etch of Shadow Trench Isolation

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**Abstract--** Shallow trench isolation (STI) planarized with chemical mechanical polishing (CMP) has replaced local oxidation of silicon (LOCOS) as the conventional isolation technique for sub-micron devices. STI increases transistor-packing density, allowing for more functionality and speed per unit area. STI offer superior latch-up immunity, smaller channel-width encroachment and better planarity. The implementation and feasibility of STI has been examined for device fabrication at RIT previously. The process utilized was etching of shallow trenches using  $\text{SF}_6\text{-O}_2$  dry chemistry and trench fill by TEOS (tetraethylorthosilicate) oxide deposition. The etch chemistry used did not yield anisotropic etching and appreciable undercutting was observed.

In the present study, STI process used includes 60 nm of thermal pad oxide and 160 nm of LPCVD nitride as the hard mask. To create the shallow trenches, Si is etched using  $\text{SF}_6\text{-CHF}_3$  chemistry for dry etching. The objective is to etch the trenches of depth  $\sim 0.5\text{ }\mu\text{m} - 0.8\text{ }\mu\text{m}$  deep without undercutting and with high selectivity on resist. A series of experiments have been done to study the Si trench etching using  $\text{SF}_6\text{-CHF}_3$  chemistry in the DryTek Quad tool by varying process parameters. The results will be presented at the conference.

## 1. INTRODUCTION

The LOCOS (LOCal Oxide of Silicon) is used as a conventional isolation technology for CMOS and BiCMOS. LOCOS geometries reach submicron size, therefore it reach the limits of effectiveness because of "bird's beak". The encroachment of the field oxide becomes significantly unacceptable large when the size of LOCOS is shrunk down to the smallest geometry devices as possible in submicron technology. Because the bird's beak extends the large encroachment into the device active regions. And another problem is that thickness of the field oxide in submicron regions. Since the thickness of the field oxide becomes significantly thinner than that grown in wider spacing of the field oxide, which create the

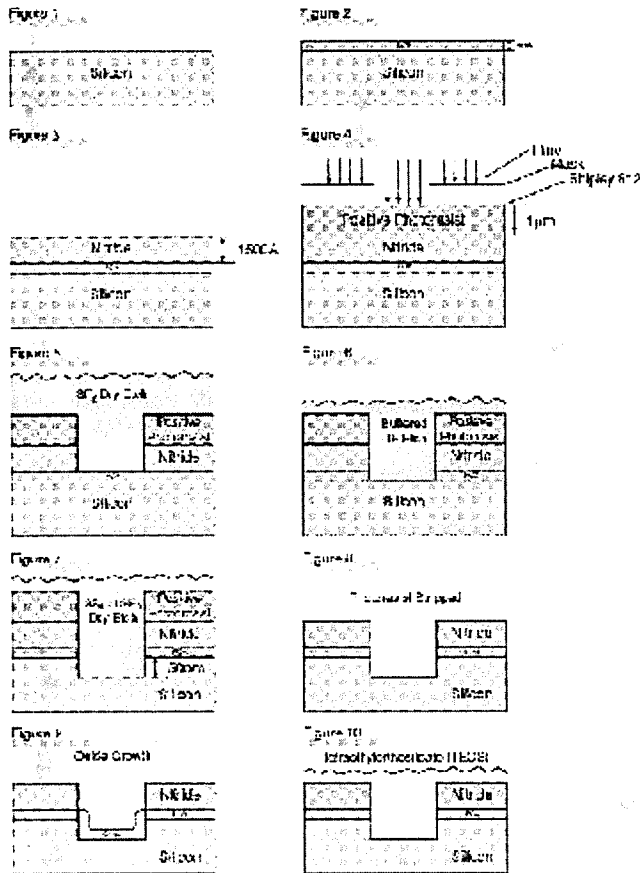
significant problem with respect to field threshold voltage and field-edge leakage. The shadow trench isolation (STI) is another isolation method in CMOS for latch up protection. Since STI is compatible to the CMOS or BiCMOS technologies, LOCOS is simply and easily replaced with STI for devices within the same tub in CMOS or BiCMOS. STI is now widely used in any semiconductor industrial to manufacture the submicron devices with STI.

After the 1500 Å nitride and 500 Å oxide layers are etched into the trench by sulfur hexafluoride ( $\text{SF}_6$ ) a dry etch, and buffered hydro fluoride (HF) wet etch, the trench in the silicon substrate is anisotropically etched between .5  $\mu\text{m}$  and .8  $\mu\text{m}$  depth by DryTek Quad with sulfur hexafluoride ( $\text{SF}_6$ ) and trifluoridomethane ( $\text{CHF}_3$ ) dry etch gas species. The sidewalls in those trenches should be smooth with an angle of 87 degree. Also the undercutting of the nitride mask should be avoided. The bottom of trench should be smooth with nice rounded corners as "U" shaped. The polymer deposition is built up by  $\text{CHF}_3$  gas. Therefore the deposited polymeric and positive photoresist films should be removed prior to annealing and refilling of the trench by ashing with dry oxygen for 45 minutes. Annealing with dry oxide at 1000°C for 45 minutes in the Bruce furnace should repair the damaged sidewalls. The thickness of dry oxide on the sidewalls and bottom of trench is about 50 nm. The refilling chemical in the trench is a tetraethylorthosilicate (TEOS) deposition process. The TEOS deposition process is done in which TEOS layer can be deposited in the trench with void-free gap fill and on the surface of nitride at lower temperature at between 350°C and 800°C. This TEOS deposition ensures a good isolation between the devices

## 2. EXPERIMENTATION

In first fabrication step, at least 500 Å thickness of pad oxide layer is grown on the top of bare silicon wafer. The recipe of dry oxide growth is uploaded into Bruce furnace system with the temperature at about 1000°C for 45 minutes from ramp up to ramp down. The dry oxygen is feeding into the furnace tube to grow the oxide layer

slowly on the surface of bare silicon wafer.



And then at least 1500 Å thickness of nitride layer is done in the low-pressure chemical vapor deposition (LPCVD) tool with a standard Nitride 1:1 recipe. The recipe is uploaded into the LPCVD system with 800°C for 27 minutes. The rate of nitride 1:1 growth is approximately 58 Å/min. The ratio of Nitride and pad oxide is 3 to 1. The nitride layer is characterized as a hard mask to resist the dry etching and as CMP stopper.

The positive photoresist (Shipley 812), as shown in Figure 4, is coated on the top of nitride layer by the GCA WaferTrac. The thickness of positive photoresist is approximately 1 µm thick. This positive photoresist thickness allows resisting the sulfur hexafluoride (SF<sub>6</sub>) and trifluoromethane (CHF<sub>3</sub>) dry etch gas species in the Dry Etch Quad system. The developer of Shipley CD-26 removes the exposed area of the photoresist coat. The patterned area is an open area where allow the dry etch to etch into the trench. The rate of 30 sccm SF<sub>6</sub> for Shipley 812 photoresist is approximately 861 Å/sec with the pressure of 300 mTorr and RF Forward power of 276 w. The etch rate of both 30 sccm SF<sub>6</sub> and 30 sccm CHF<sub>3</sub> for the same photoresist is about 1175.17 Å/min.

The trench of nitride is etched with 30 sccm SF<sub>6</sub> dry

etch in DryTec Quad system for about 44 seconds with low pressure of 300 mTorr and RF Forward power of 276 watt as shown in Figure 5. The etch rate is approximately 2480 Å/min.

The layer of oxide would slow the dry chemical etching down and is being etched isotropically by the dry etching, therefore there is a different kind of solution to etch the oxide layer faster. The layer of oxide is removed by Buffered HF, a wet etch solution, for approximately minutes as shown Figure 6. The characterization of wet etch solution is a true isotropic etch.

Etching the .5 µm-.8 µm silicon trench is done with a gas mixture of 30 sccm SF<sub>6</sub>, and 30 sccm CHF<sub>3</sub> gas species, which produces very large concentrations of free fluoride, F, as shown in Figure 8. In the low pressure environment at 65 mTorr, the ion bombardment of fluoride with 267 w RF Forward is a characterization to etch the silicon, because silicon is quite attracted to fluoride, and the methane, CH<sub>4</sub>, is a polymerization that the film is created to passivate the sidewalls, preventing lateral etching.

After the dry etching in silicon trench is done, ash removes the polymeric films such as positive resist and CH for 45 minutes. Acetone is used to remove those polymeric residual in the trench and surface.

After 45 minutes annealing process with 1000° C of dry oxide is required for repairing the damaged surface of sidewalls and bottom of trench, the Tetraethylorthosilicate (TEOS) is injected to deposit SiO<sub>2</sub> into the shadow trench isolation at approximately 400°C for couple minutes as shown in Figure 10. Thickness of TEOS is required to be about at least 1500 Å for the planarization.

### 3. EXPERIMENTAL RESULTS

**Nitride etch:** The etch rate for the nitride is about 2465.4 Å/minute. The nitride layer is entirely etched into trench for about 40 seconds in DryTek Quad Chamber. The RF Forward is approximately 276 watt. The pressure in the chamber #2 is 300 mTorr. The gas flow dispensing in the chamber is about 30 sccm SF<sub>6</sub>. The green color of nitride is disappeared after dry etching is performed. The photoresist layer is remained the same, but the thickness is reduced from 1 µm to about .94 µm. The SF<sub>6</sub> etch rate for positive photoresist is approximately 14.35 Å/second.

**Oxide etch:** The layer of 600 Å dry oxide is removed entirely. The tan color for oxide is disappeared in the trench regions by buffered hydro fluoride. After the wet etching, the measurement of oxide thickness is less than 20 Å as it is revealed by Nanospec instrument.

**Silicon etch:** the etch time increment is about 10 seconds for each run. The etching time for the first run is 140 seconds. The etching time for the last run is about 180 seconds. The pressure in the chamber #2 is 65 mTorr, the pressure setting is remained the same for every run. The RF Forward is 276 watt for every wafer. The gas flow for this mixture gas contains 30 sccm  $\text{SF}_6$  and 30 sccm  $\text{CHF}_3$  gases. The etch rate of gas mixture for silicon trench is about 55.38 Å/second. The etch rate for silicon trench ranges from 42.5 Å/second to 71.81 Å/second. The etch rate for the photoresist ranges from 32.39 Å/second to 65.35 Å/second. The etch ratio of photoresist ranges from 1:1.27 to 1:1.50. The most photoresist thickness is remained on the surface of nitride.

**Trench sidewalls:** The images from SEM show that those sidewalls are some curve and straight as steep. "Over-annealing" with very high temperature and very long time caused to create some curve walls. The length of temperature and time of annealing should be about 1000<sup>o</sup> C and 45 minutes in dry oxide furnace. The device #14 looks very good comparing with other devices. The device #14 is about .5  $\mu\text{m}$  depth of silicon trench as shown in Picture 1.

**Trench bottom:** The trench bottom corners are very rounded corners as shaped "U". They look very excellent shape of trench bottom as shown Picture 1, 2, 3, and 4.

**Chemical Filling:** The TEOS chemical filling is substituted to LTO filling due to the contaminated LPCVD tube #15. The LTO or TEOS experiment is not intended to use for dry etch studying. Chemical filling is merely used for observation in x-section results. The TEOS filling is a standard for STI technology in semiconductor industrials. The LTO chemical depositing rate in the trench and on the surface is about 100 Å/minutes. LTO depositing time for STI in LPCVD for approximately 2.5 hours at 425<sup>o</sup> C. The measurement of LTO thickness on the monitor wafer is about 15000 Å. It was measured by ellipsometric instrument.

#### 4. CONCLUSION

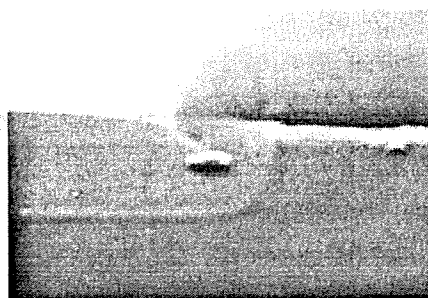
The trench sidewalls is possibly an evidence of the etch profile of silicon trench, that may suppresses the polymeric formation with high concentrations of  $\text{SF}_6$  and  $\text{CHF}_3$  gas species, and the characterization of etch profile is isotropic with substantial "undercut" of the mask as shown in Picture 2, 3, and 4. The result of device 14 of .5  $\mu\text{m}$  silicon trenches, as shown in Picture 1, looks better than the rest of other STI results.

The aggressive gas mixture of  $\text{SF}_6$  and  $\text{CHF}_3$  species quickly and wholly devoured the nitride layer in a minute

in range from 100 mTorr to 300 mTorr. The nitride layer does not do well in masking against dry etching. The photoresist of 1  $\mu\text{m}$  thickness is placed to stay on the top of nitride layer for this gas mixture etching. The nitride is for the CMP stopper. It is designed to stop the polishing from destroying the surface of device and isolation.



Picture 1 .51  $\mu\text{m}$  Silicon Trench



Picture 2 .93  $\mu\text{m}$  Silicon Trench



Picture 3 .87  $\mu\text{m}$  Silicon Trench



Picture 4 .72 um Silicon Trench

#### 4. FUTURE WORK

The gas mixture of  $\text{SF}_6$  and  $\text{CHF}_3$  may need adjusted in various size of gas concentration in the order to be achieved in a pure anisotropic dry etching without suppressing the polymeric formation or the annealing setting may be adjusted in temperature and time to improve the sidewall and reduce the "curve" wall. Predicting etch rate is enhanced by controls some certain parameters such as temperature, concentration, pressure, and RF forward power. The RF power supply will have to be replaced since it behaves crazy and it does not keep those DC Bias, RF Forward, and other parameters stabilized. The DryTec Quad apparently does not have the temperature controlling such as coolant system to keep the temperature in constant.

#### REFERENCES

- [1] Daewon Ha et al. "Anomalous Junction Leakage Current Induced by Sti Dislocations and Its Impact on Dynamic Random Access Memory Devices" IEEE Transactions On Electron Devices, Vol. 46, No. 5, May 1999 p. 940
- [2] Nag. S. et al. "Comparative Evaluation of Gap-Fill dielectrics in Shallow Trench Isolation for sub 0.25 um Technologies" Tech dig IEDM 1996 p 841
- [3] T. Curtis, et.al, "APCVD TEOS Ozone thin film integration for Multilevel
- [4] Mikoshiba. H. et al." A New trench Isolation as a replacement of LOCOS." Tech. Dig IEDM. 1984 p. 578
- [5] "Gaining control over STI process ". Semiconductor International Jan 2000
- [6] Jai-hoon Sim et al. "High-Performance Cell Transistor Design Using Metallic Shield Embedded Shallow Trench Isolation (MSE-STI) for Gbit Generation DRAM's." IEEE Transactions On Electron Devices, Vol. 46, No. 6, June 1999 p. 1212
- [6] " Wide margin CMP for STI" Solid State Technology , July 1998 volume 41 , issue 7
- [7] S.S. Cooperman, A.L. Nasr, G.J. Grula, "Optimization of a shallow Trench Isolation Process For improved

Planarization" J. Electrochemical. Soc., Vol 142, no. 9. pp. 3180-3185 , Sept 1995

[8] "CMP dishing effects in Shallow Trench isolation" July 1997, volume 40, issue 7

[9] " Improved planarization for STI with fixed abrasive technology " Solid State Technology June 2000, volume 43, issue 6

[10] M. Nandakumar, et.al., "Shallow Trench Isolation for advance ULSI CMOS Technologies" 1998 IEDM TECH.

[11] Chen. C. et al. "A novel 0.25 um Shallow trench isolation Technology." Tech. Dig. IEDM 1996 p. 837

[12] Shih-Chia Lin. et al. "A Closed-Form Back-Gate-Bias Related Inverse Narrow-Channel Effect Model for Deep-Submicron VLSI CMOS Devices Using Shallow trench isolation Technology." IEEE Transactions On Electron Devices, Vol. 47, No. 4, APRIL 2000 p. 725

[13] Toshiyuki Oishi. et al. "Isolation Edge Effect Depending on gate Length of Mosfet's with Various Isolation Structures" IEEE Transactions On Electron Devices, Vol. 47, No. 4, APRIL 2000 p. 822

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# CMP Process Development for Shallow Trench Isolation (STI)

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**Abstract**—Tool characterization and optimization was performed on a Westech Model 372 Polisher. A Rhodes ESM-U pad with a #5 groove with PSA and two slurries: a Rodel Klebosol 1501-50 silica based slurry and a proprietary cerium oxide slurry were utilized. Initial polishing of blanket thermal oxide wafers on the Westech produced %WIWNU greater than 80% using the Klebosol slurry. Following tool calibrations and modifications to machine configurations, %WIWNU dropped to approximately 5%. Characterization studies were performed for Removal Rate vs. Platen RPM and for Removal Rate vs. Down Force. An increase in removal rate was determined with an increase in platen RPM while a linear relationship between removal rate and down force existed. Blanket nitride and low temperature oxide (LTO) wafers were polished using both silica and ceria slurries to determine removal rates. Oxide to Nitride Selectivity for the Klebosol slurry was 4:1 while the ceria slurry was 100 times more selective. STI structures were manufactured and polished. Trench dishing was studied using Alphastep measurements. Severe dishing was observed with the silica based slurry. The ceria slurry produced no dishing effects.

## 1. BACKGROUND

As design rules shrink and microprocessor speeds increase, the ability to isolate devices becomes more and more important. A transition from LOCOS (Local Oxidation of Silicon) to Shallow Trench Isolation (STI) is needed for scaling beyond 0.25  $\mu\text{m}$ . STI dramatically shrinks the area needed to isolate transistors while offering more functionality, more speed per unit area, superior latch-up immunity, and better planarity. However, the more complex STI process creates challenges in providing void-free CVD films, sloped etch profiles, and uniform planarization by CMP.

STI structures represent CMP's newest and most important application for device-level processing. The mainstream implementation of STI throughout the semiconductor has taken place throughout industry. Currently, STI processing is unavailable at the Rochester

Institute of Technology. The purpose of this project was to develop and optimize a CMP process for future STI applications at RIT. This was achieved by identifying appropriate CMP consumables for current STI processes. Both silica and ceria based slurries were investigated. Removal rates, oxide-to-nitride selectivity, and uniformities were determined to be a function of process parameters and materials. SEM pictures and Alphastep measurements were utilized to determine the effects of trench dishing.

## 2. EXPERIMENTAL

Initial tool training was given on the Westech Model 372 Polisher by Bruce Tolleson. Two issues with the CMP tool were discovered during this session. The first issue was the inability to flow DI water to the primary platen. The other problem was the slurry flow was not calibrated. A setting of 100mL/min corresponded to an actual flow of 149mL/min.

The pad that would be used on the Westech Model 372 Polisher was a Rhodes ESM-U. Rhodes is a division of Universal Photonics. The pad had a thickness of 0.1" and a groove depth of 0.050". The groove pattern was an x-y pattern with 5mm islands and the groove width was 1mm. This pad is very similar to the IC1000/SubaIV with a k-groove manufactured by Rodel. Two slurries were utilized during the experimental section of this project. The first slurry was a Klebosol 1501-50, silica based slurry manufactured by Rodel. The second slurry was proprietary cerium oxide slurry.

Lot #1 consisted of twenty-five 4" monitor wafers and were scribed Drew1 EMCR690 to Drew25 EMCR690. These wafers will be used for STI structures. The structures that were constructed on these wafers resembled STI-structures, however, the silicon trench etch were not performed on these wafers. The silicon trench for Shallow Trench Isolation was being development and optimized by another student, Patrick Reese. Thus, the structures created to characterize and optimize a CMP process for STI were referred to as STI-like structures.

The processing steps for the STI-like structures are as follows:

1. RCA Clean
2. Pad Oxide Growth (500Å)
3. Nitride Deposition (1600Å)
4. Pattern Nitride with CMP Test Mask
5. Nitride etch (DryTech Quad)
6. LTO Deposition (5500Å)
7. LTO Densification

The RCA clean used was the standard recipe used at RIT. The pad oxide growth took place in the Bruce Furnace using Recipe #250. Thickness measurements were verified using the Nanospec. The nitride growth was performed in lower tube of the 6" LPCVD furnace. The nitride film deposited was a 1:1 ratio of ammonia to dichlorosilane. The deposition time for a thickness of 1600Å was 29 minutes. Nitride thickness measurements were performed on bare Si test wafers using the Nanospec. The nitride film was then patterned using CMP Test Mask. Standard coat and develop recipes were used on the 4" Wafertrac. Exposure was performed on the GCA stepper using recipe Ricky. The nitride film was then etched using the DryTech Quad. The settings for this etch are as follows: 30sccm of SF<sub>6</sub> (gas flow), 300mTorr (pressure), 267W (Power), and a etch time of 2 minutes. The resist was ashed using the ozone asher for 45 minutes. The LTO deposition was performed in the upper tube of 6" LPCVD furnace. The recipe used was the standard 425°C LTO for a deposition time of 60 minutes. LTO densification was performed in Tube 14 of the mechanical furnace. The wafers were exposed to an O<sub>2</sub> ambient for 2 hours.

Twenty-five 4" monitor wafers were used for initial polishing and tool characterization. These wafers underwent a RCA clean prior to a one-micron thermal oxide growth in tube 4 of the Bruce Furnace. This group of wafers was Lot #2 and were scribed Drew26 EMCR690 to Drew50 EMCR690.

Another lot of twenty-five 4" monitor wafers were used for blanket nitride and low temperature oxide (LTO) wafers. Nitride and LTO films were deposited by use of the 6" LPCVD and recipe specifications were the same as those previously mentioned for STI-like structures. A pad oxide of 500Å was grown on the nitride wafers before nitride deposition. These wafers were Lot #3 and were scribed Drew51 EMCR690 through Drew75 EMCR690. Wafers Drew51 EMCR690 through Drew63 EMCR690 were used for blanket nitride wafers and the remaining wafers were utilized for blanket LTO films.

Additional tool repairs and operator training were performed before the initial polishing on the Westech CMP tool began. Wafer Drew26 was first wafer polished on the Westech Model 372 Polisher. Additional blanket thermal oxide wafers were polished on the tool to study uniformity issues. Tool calibrations and modifications to

machine configurations were performed. A %WIWNU study was performed using blanket thermal oxide wafers to determine optimum tool settings. Additional tool characterization was performed by a Removal Rate vs. Platen RPM and Removal Rate vs. Down Force studies.

Blanket nitride and LTO wafers were polished using both silica and ceria slurries. Removal rates and selectivities were determined. STI-like structures were also polished using both silica and ceria slurries. Optical images were used to compare structures before and after CMP. Trench dishing measurements were performed using the Alphastep. SEM images were also taken on wafers polished using the silica slurry. Wafers polished using the ceria slurry were unable to be SEM'ed due to inadequate slurry removal procedures.

### 3. RESULTS AND DISCUSSION

The first wafer polished on the Westech Model 372 Polisher was very non-uniform. There were many hot spots on the wafer where all the oxide was completely removed. The non-uniform polish can be attributed to problems with the tool sensing pressure. The pressure readout on the tool varied from 1PSI to as high as 10.5PSI. Figure 1 and Figure 2 show a 1µm thermal oxide wafer before and after CMP. The wafer was polished for one minute using a down force of 4PSI, a slurry flow of 30mL/min, a Platen RPM of 32RPM, a Carrier RPM of 28 RPM, and Rodel Klebosol silica based slurry.

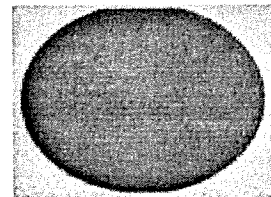


Figure 1: 1µm thermal oxide wafer before CMP



Figure 2: 1µm thermal oxide wafer after CMP

Down force calibrations were performed to make sure the applied down force was equal to the pressure readout on the Westech Polisher. Troubleshooting was performed on the tool and constant pressure readings were finally achieved. Modifications to the machine configuration were also performed. Figure 3 shows a thermal oxide



wafer polished after tool calibrations using the same settings as the wafer polished in Figure 2.

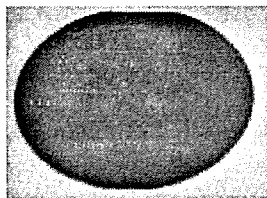


Figure 3: 1μm thermal oxide wafer after CMP and tool calibrations

Tool characterizations studies were performed to determine the optimum tool settings that yield the lowest %WIWNU. The ideal settings were a Platen RPM of 40RPM and a down force of 4PSI. Slurry flow and platen RPM were kept constant at 30mL/min and 28RPM, respectively. Figure 4 is a plot of uniformity across the wafer for various RPMs: Wafer #31-50RPM, Wafer #32 – 40RPM, and Wafer #33 – 30RPM. Wafer #30 is a 1μm thermal oxide wafer before CMP.

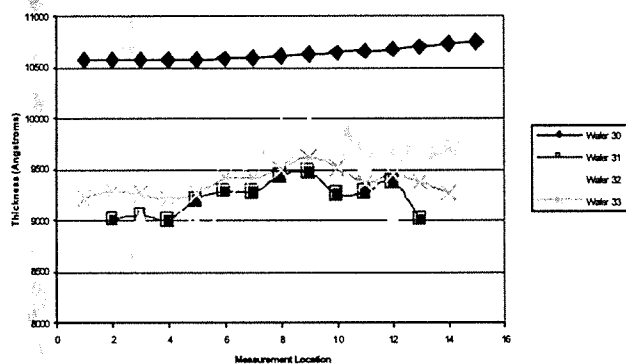


Figure 4: Thickness across the wafer (Across the diameter of the wafer, minor flat to major flat)

Removal rate versus Platen RPM was also studied. It was determined that the removal rate increased with an increase in Platen RPM. This corresponds to Preston's Equation, which is listed below:

$$\text{Polish Rate} = K_p P (\Delta s / \Delta t)$$

Thus, the equation states as the linear velocity increases relative to the workpiece, the polish rate will also increase. Figure 5 is a graph of Removal Rate versus Platen RPM.

Removal Rate vs. Platen RPM

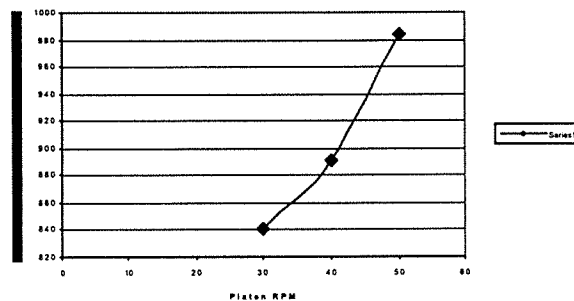


Figure 5: Removal Rate vs. Platen RPM

Removal rate versus down force was studied to test that an increase in down force corresponds to an increase in removal rate. A linear relationship between removal rate and down force existed and can be seen in Figure 6.

Removal Rate vs Down Force

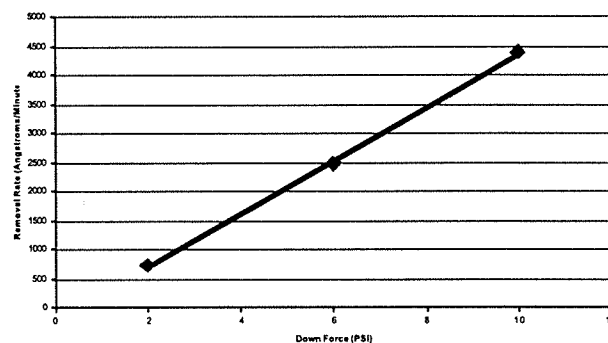


Figure 6: Removal Rate vs. Down Force

Blanket nitride and LTO wafers were polished using the Rodel Klebosol slurry and the proprietary ceria slurry to determine removal rates. These wafers were polished using the following parameters:

- Down Force: 4PSI
- Slurry Flow: 30mL/min
- Platen RPM: 50 RPM
- Carrier RPM: 28 RPM
- Polish Time: 1.5 minutes

Results for nitride and LTO polishing are listed in Table 1.

Table 1: Removal Rates and Selectivity for LTO and Nitride blanket wafers using Silica and Ceria Slurries

	Silica Slurry	Ceria Slurry
LTO Removal Rate	1990Å/minute	595Å/minute
Nitride Removal Rate	485Å/minute	1.5Å/minute
Selectivity (Oxide: Nitride)	4:1	400:1

The ceria slurry was 100 times more selective than the silica slurry.

STI-like structures were polished using both silica and ceria slurries using the following parameters:

- Down Force: 4PSI
- Slurry Flow: 30mL/min
- Platen RPM: 40 RPM
- Carrier RPM: 28 RPM
- Polish Time: Dependent on Removal Rate

Trench dishing was evaluated by the use of Alphastep measurements. The silica based slurry produced very severe dishing while the ceria slurry exhibited no dishing effects. The dishing effect was affected greatly by the selectivity of the slurry used and by the type of feature polished. The effects of trench dishing are illustrated in Figures 7, 8, and 9. Figure 7 illustrates 5µm lines and 45µm spaces before CMP. Figures 8 and 9 show the effects of trench dishing on 5µm lines and 45µm spaces after CMP using a silica and ceria slurry, respectively.

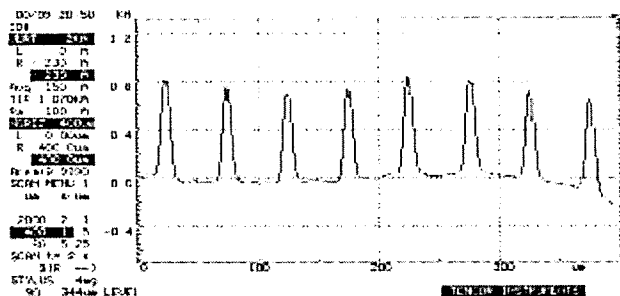


Figure 7: 5µm lines and 45µm spaces; Before CMP

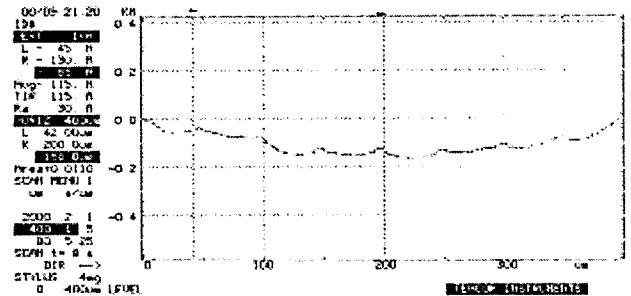


Figure 8: 5µm lines and 45µm spaces; After CMP w/ Silica Slurry

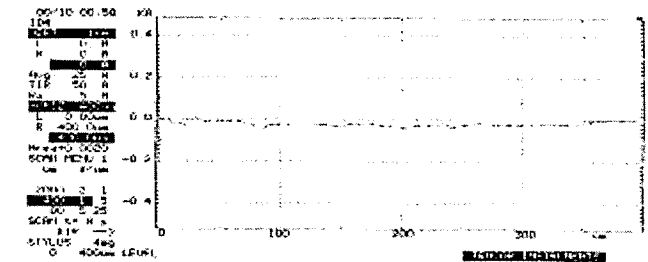


Figure 9: 5µm lines and 45µm spaces; After CMP w/ Ceria Slurry

## 4. CONCLUSIONS

The development of CMP process for Shallow Trench Isolation was a success. The base CMP process can be applied to future STI applications at the Rochester Institute of Technology. The ceria based slurry produced oxide to nitride selectivities of 400:1 and produced no dishing effects while using a Rhodes ESM-U pad. Future work using the Westech Model 372 Polisher can be performed in the areas of endpoint detection, slurry and pad characterization, and down force pressure optimization.

## REFERENCES

- [1] Trench Warfare: CMP and Shallow Trench Isolation; <http://www.semiconductor-intl.com/semiconductor/issues/issues/1999/oct99/docs/feature5.asp>
- [2] Gaining Control over STI Processes; <http://www.semiconductor.net/semiconductor/issues/issues/2000/200003/six003sti.asp>
- [3] Choices and Challenges for Shallow Trench Isolation; <http://www.semiconductor.net/semiconductor/issues/issues/1999/apr99/docs/feature2.asp>

## ACKNOWLEDGMENTS

The author acknowledges Dr. Mike Jackson for guidance during the CMP process development, Dr. Richard Lane for CMP theory, and Dr. Santosh Kurinec for STI processing. Additionally, the author would like to thank Bruce Tolleson for equipment support for the Westech Model 372 Polisher, David Yackoff for equipment support on the Bruce Furnace and LPCVD system, Jose Medina for SEM work, and Nate Westcott and An Pham for processing knowledge.



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# Polysilicon-Germanium Films Fabricated by Ge Sputtering

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**Abstract**— Poly-Si<sub>x</sub>Ge<sub>1-x</sub> films were fabricated on 500 Å of oxide by a novel process. Values for X range from 0.86 to 0.45. This novel process consists of two steps as opposed to the single step polysilicon-germanium deposition methods currently used in industry. Ge was deposited by PVD and polysilicon was deposited on top of the germanium by LPCVD in a silane ambient. The films were doped P<sup>+</sup> with boron dopant and annealed at 1,000°C for 50 minutes in a nitrogen ambient. Films with 65 and 55% Ge suffered from voids and hillocks and film discontinuity. Films with 20 and 14% Ge were relative smooth compared to the films with a high percentage of Ge. Standard polysilicon films yield a sheet resistance of 59.01 ohm/square while films with 20 and 14% Ge yield values of 44.71 and 41.41 ohm/square respectively.

## I. INTRODUCTION

As the semiconductor industry approaches deep sub-micron device regime more challenges are being encountered in the fabrication of such small devices. To make symmetric n- and p- channel devices, dual gate approach becomes necessary i.e. n+ polygate for NMOS and p+ polygate for PMOS devices. As the devices are shrinking in lateral dimensions so are the vertical dimensions. Gate oxide has already reached ~ 2 nm in thickness. Boron penetration into the thin gate oxide from the p+ polygate has become a serious problem[2]. This is illustrated in Figure 1. If boron is kept away from the oxide-poly interface, it gives rise to gate depletion effect (GDE)[2]. The gate region close to the interface goes into depletion causing extra capacitance and effective reduction of gate voltage and drive current. This is illustrated in Figure 2. Polysilicon-germanium films have been proposed as potential replacement for conventional polysilicon gates. Various film compositions of polySi<sub>x</sub>Ge<sub>1-x</sub> have been suggested, all with promising results[1][2][3][4]. This material requires lower temperature for dopant activation, which reduces boron penetration yielding better gate oxide reliability, decreases thermal budget and processing time. PolySi<sub>x</sub>Ge<sub>1-x</sub> is usually deposited by Low Pressure Chemical Vapor Deposition (LPCVD) with the use of Silane, SiH<sub>4</sub>, and Germanium, GeH<sub>4</sub> gases.

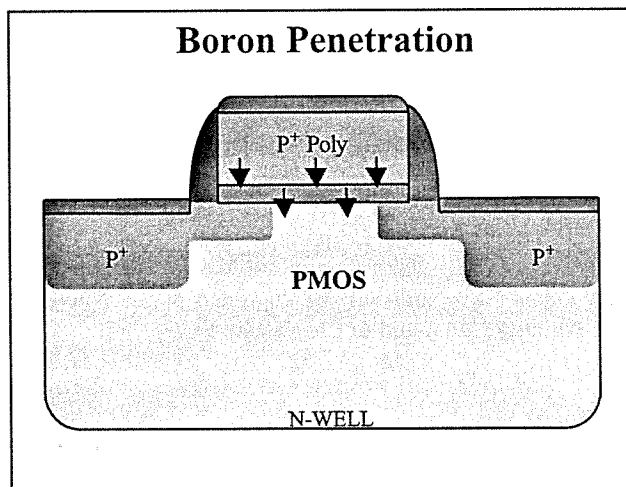


Figure 1

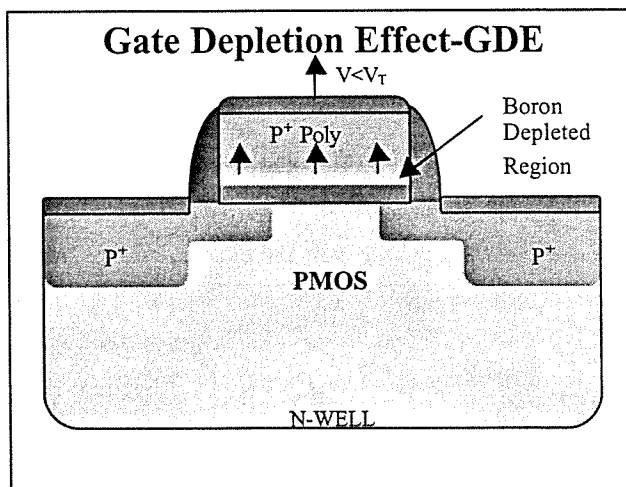


Figure 2

In this investigation, polysilicon-germanium films have been fabricated by depositing LPCVD polysilicon on PVD germanium films. Germanium films were deposited from a four-inch target in a sputtering system and polysilicon was deposited using silane gas in a LPCVD furnace. During the polysilicon deposition and the subsequent anneal after the doping of the film, the two

films are expected to react to form  $\text{polySi}_x\text{Ge}_{1-x}$ . The films were doped with boron and annealed at 1,000°C. Polysilicon-germanium composition and resistivity will be studied and compared to standard polysilicon films.

## II. EXPERIMENT

The first step in the two-step process of fabricating polysilicon-germanium films by Ge sputtering is to deposit Ge. A process to deposit Ge by PVD was generated and optimized using a CVC601 sputtering tool and a 4" germanium target. To obtain a desired Ge thickness of 1,500 Å, the deposition time was set to 20 minutes, the power was set to 200 Watts and the argon flow was set to 56.5 sccm yielding a sputtering pressure of 5 mTorr. The second step in this two-step novel process is to deposit polysilicon using a LPCVD tube with a silane ambient. A 6,000 Å polysilicon film was deposited on top of the 1,500 Å of Ge using RITs standard polysilicon recipe for their PW-3 CMOS process. A  $\text{polySi}_{0.80}\text{Ge}_{0.20}$  film was achieved with this process. A  $\text{polySi}_{0.86}\text{Ge}_{0.14}$  film was fabricated by depositing a 2,700 Å LPCVD polysilicon film before this novel process was started. The deposition time in the sputtering tool was increased to fabricate the films with a high percentage of Ge. All samples were doped  $\text{P}^+$  with boron dopant and annealed at 1,000°C for 50 minutes in a nitrogen ambient. Film microstructures were examined in a 501 Phillips SEM at 320X and 10,000X magnifications. Sheet resistance of the films was measured at the five standard points of interest used at RIT during routine inspections.

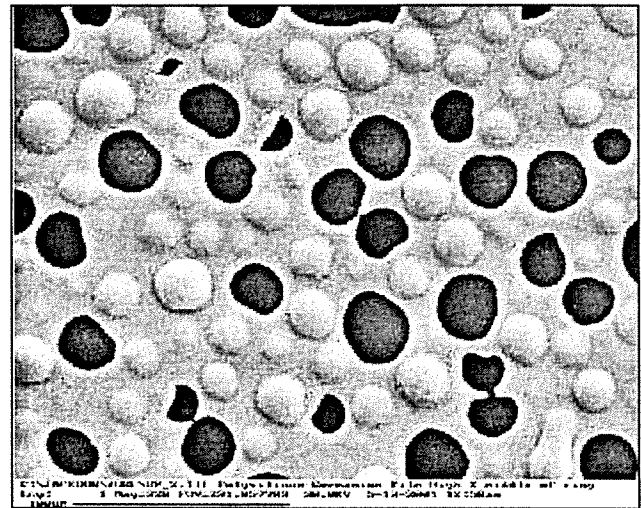
## III. RESULTS AND DISCUSSION

Usual percentages of germanium in Polysilicon for industry do not exceed 35%. In this experimentation the fabrication of films with a relatively high Ge concentration, 65 and 55%, produce reasons as to why the germanium concentration in a polysilicon film must be low. Films with 65 and 55% Ge suffered from voids and hillocks and film discontinuity. This is illustrated in Micrograph 1 and 2. The discontinuity of polysilicon-germanium films with high Ge concentrations due to voids and hillocks makes this film unusable in the semiconductor industry. Films with 20 and 14% Ge were relative smooth compared to the films with a high percentage of Ge. This is illustrated in Micrograph 3 and 4. These films are ideal for IC manufacturing since a continuous signal can be sent through wires made with this material. Another reason for the ideality of these films smoothness would be the decrease in resistance achieved as a result of reduced film discontinuity. Standard polysilicon films yield a sheet resistance of 59.01 ohm/square while films with 20 and 14% Ge yield values of 44.71 and 41.41 ohm/square respectively. From these results the decrease of sheet

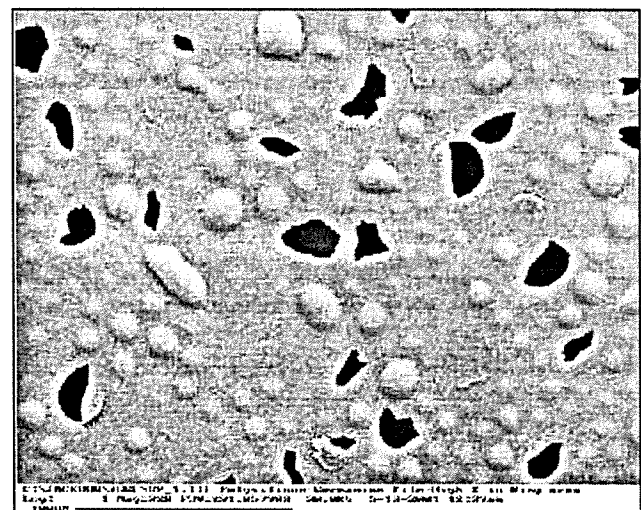
resistance as a result of the introduction of germanium into these films is proven. Table 1 summarizes the film thickness, Ge percentage and sheet resistance values obtained throughout this investigation.

Film Composition and Sheet Resistance			
Film	Thickness (Å)	Ge (%)	Rs (ohm/square)
Polysilicon	6000	0	59.01
Poly/Ge	6000/1500	20	44.72
Poly/Ge/Poly	6000/1500/2700	14	41.41

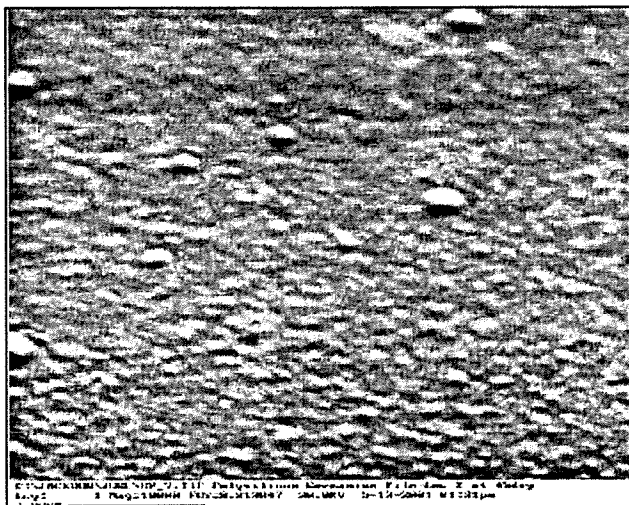
Table 1: Summarized results.



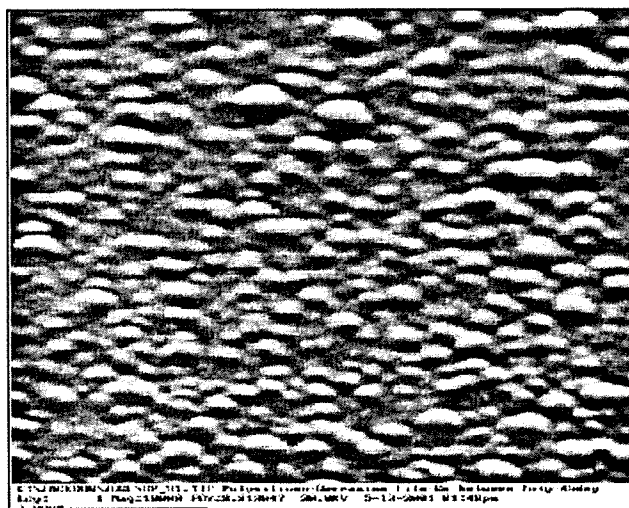
Micrograph 1: Polysilicon-Germanium film after anneal with a Ge concentration of 65% taken at a magnitude of 320X.



Micrograph 2: Polysilicon-Germanium film after anneal with a Ge concentration of 55% taken at a magnitude of 320X.



Micrograph 3: Polysilicon-Germanium film after anneal with a Ge concentration of 20% taken at a magnitude of 10,000X.



Micrograph 4: Polysilicon-Germanium film after anneal with a Ge concentration of 14% taken at a magnitude of 10,000X.

#### IV. CONCLUSION

Polysilicon-germanium films have been successfully fabricated at RITs Microelectronic Engineering Laboratory by Ge sputtering. Films with low percentages of Ge demonstrated desirable film microstructures with potential for use in microelectronic devices. Lower sheet resistance was obtained when adding Ge to standard polysilicon films. A reduction of 25% in sheet resistance for films with 20% Ge was achieved. For films with 14% Ge, a reduction in sheet resistance of 35% was achieved. Another possible reason for the improvement in sheet resistance for the films with 14% Ge would be that Ge was in between polysilicon films possibly creating a better distribution of Ge in polysilicon. Future work to be done as a

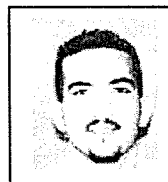
continuation of this investigation is to study the Ge profile in polysilicon after LPCVD poly deposition, to study the boron profile in polysilicon-germanium after anneal, to study effects on boron activation of time and temperature during anneal and to incorporate an optimized process to fabricate these films into PMOS devices to study its electrical properties when testing a device.

#### REFERENCES

- [1] Wen-Chin Lee, Bryan Watson, Tsu-Jae King, and Chenming Hu, "Enhancement of PMOS Device Performance with Poly-SiGe Gate," IEEE Electron Device Letters, Vol. 20, No. 5, May 1999
- [2] Wen-Cin Lee, Tsu-Jae King, and Chenming Hu, "Optimized Poly-Si<sub>1-x</sub>Ge<sub>x</sub>-Gate Technology for Dual-Gate CMOS Application," Proc. Symp. VLSI Technology, Honolulu, HI, June 1998
- [3] Hellberg, P.-E.; Zhang, S.-L., "Polycrystalline p<sup>+</sup>-Si<sub>x</sub>Ge<sub>1-x</sub> as a single gate in CMOS technology," Physica Scripta Volume T, vol.T79 p. 225-7
- [4] King, T.-J.; Pfister, J.R.; Shott, J.D.; McVittie, J.P.; Saraswat, K.C., "A polycrystalline-Si<sub>1-x</sub>Ge<sub>x</sub>-gate CMOS technology," International Electron Devices Meeting 1990. Technical Digest p. 986, 253-6

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# The Effect of Fluorine on Low Temperature Boron Activation in Ultra Shallow Junctions

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**Abstract--** As CMOS device dimensions continue to shrink below 200nm, one of the major limiting factors in scaling size will become the drain and source junction depth. Using fluorine to create shallower p-type junctions during ion implant is one way to decrease the junction depth. The effect of fluorine on the implant and subsequent anneal processes was studied. A low temperature annealing process was developed to decrease junction depths although sufficient dopant activation is being studied.

## 1. INTRODUCTION

Critical dimensions of CMOS transistors continue to shrink well below 200nm, with current processes producing gates as low as 130nm. While microlithography has been a major limiting factor in the scaling of transistors, another has been the drain/source junction depth. The junction depths must be scaled accordingly with the channel width to avoid undesirable short channel effects such as threshold voltage roll off and punchthrough. Current processing requires a drain junction depth ( $X_j$ ) of 450-900Å with a sheet resistance of 200-700  $\Omega/\text{sq}$ . [1] These requirements pose very serious problems to the processes, which have begun to rely heavily on rapid thermal processing such as spike annealing to replace the slower diffusion processes which result in deeper junctions. Newer forms of doping are also being studied, including plasma doping and high-energy recoil implants. These two solutions may provide long-term revolutionary answers to doping issues, but using diffusion in a different fashion may provide a short-term solution.

Low energy ion implantation is presently the method of choice for the formation of source/drain junctions. On the other hand, ion implantation creates defects, giving rise to unwanted effects such as dopant clustering and transient enhanced diffusion (TED). The problem for making shallow boron doped p+ junctions is more severe because of higher boron ion implantation projected range and higher TED effects. Boron is usually introduced by implanting BF<sub>2</sub> that causes amorphous layer damage that allows recrystallization through solid phase epitaxy (SPE). The temperature-time product of post

implantation anneal is desired to be kept low. Reducing anneal times is possible with rapid thermal processing (RTP) by ramping temperature to the target temperature and cooling down faster, approaching a spike shaped anneal temperature-time profile. The damage produced by an implant causes a large enhancement in the diffusion coefficient of dopants, until such time as the damage is completely repaired. Experimental findings have shown that the point defects responsible for TED are interstitial type extended defects in the form of {311} clusters. The balance between cluster growth and evaporation determines the enhancement in diffusivity observed during TED. It has been suggested that at lower temperatures, the supersaturation in point defect levels is high, and excess defects remain longer due to the lower interstitial diffusion coefficient, leading to greater motion of dopants. The role of fluorine on the TED of boron is not fully understood

Experimentation was done on wafers implanted at Texas Instruments on an Applied Materials XRLeap Implanter, which is capable of low-energy implants without the use of a deceleration mode. Five sets of wafers were implanted, each with a different variation on a boron or BF<sub>2</sub> implant. These wafers were then sent to RIT for continued processing. The wafers sent to RIT were as follows:

Wafer	Implant	Energy
2	5E14 BF <sub>2</sub>	10KeV
6	1E15F/5E14B	3.9KeV/2.2KeV
10	5E14F/5E14B	3.9KeV/2.2KeV
13	5E14B	2.2KeV
16	5E14B/1E15F	2.2KeV/3.9KeV

**Table 1: Wafer Process Description**

Results for the experiment come from various sources, including a standard four-point probe system at RIT and Texas Instruments. Also used were Secondary Ion Mass Spectroscopy (SIMS) and Spreading Resistance Profiling (SRP). SIMS results show the distribution of dopant atoms (Both B11 and B10) through the use of an oxygen beam that cuts into the wafer. This test is an accurate way to measure the number of atoms present in

the wafer, but does not show the amount of dopant atoms that have been activated through annealing. SRP analysis is a two-probe measurement tool stepped across a beveled edge of the wafer, used to calculate the active dopant concentration and consequently the sheet resistance of the junction.

Use of the SRP system in ultra-shallow junctions (USJ) is difficult due to several phenomena. Using a standard SRP system for USJ processes often results in abnormally high sheet resistance calculations. The high sheet resistance is commonly attributed [2] to surface damage introduced by the beveling process. Wolf et al. have developed a low-weight SRP system using a single probe called nano-SRP which also uses an Atomic Force Microscope to produce quality SRP measurements on USJ wafers. In a standard SRP system, the probes in contact with the wafer actually produce a series of small micro-contacts. However, when SRP was developed, it was intended for use over structures tens or hundreds of microns thick, and the micro-contact effect could be easily neglected with no effect on the readings. However, as Clarysse and Vandervorst show [3], with shrinking junctions, this effect can no longer be ignored. Clarysse et al [4] also show an effective surface and equipment preparation strategy for electrically characterizing USJ profiles.

## 2. EXPERIMENTAL SETUP

The wafers sent to RIT, outlined above, were cleaved into 12 pieces to be annealed using a low temperature process taking advantage of solid phase epitaxy to activate the dopant without the added diffusion that is associated with high temperature activation. The resulting profile should be a shallow junction with as little depth added post-anneal as possible. One segment of each wafer was loaded into RIT's Bruce Diffusion furnace for each of 12 different anneals. The anneal recipes used diffusion times of 4,6,8, and 10 hours at temperatures of 400, 600, and 800°C. All anneals were done in an inert nitrogen ambient. The processes were set up so that the furnace would ramp up to temperature and stabilize before the wafers were pushed in. This process allowed the wafers to be in the furnace at a constant temperature at all times. It also allowed the recipes to be set up without needing to account for differences in ramp times. The temperatures used were low enough so the wafers were pulled out of the furnace at temperature without causing warpage.

The segments were measured using four-point probe analysis following the anneal process. The Alesi Industries four point probe uses a probe spacing of .0625" and all measurements were based on a current of 1mA, which was decided on through previous experimentation.

## 3. Results and Discussion

The results of the four-point probe measurements are as follows:

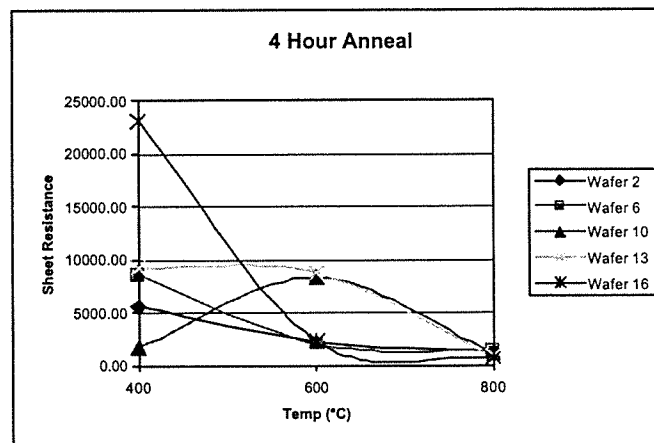


Figure 1: Sheet Resistance as a function of annealing temperature

This chart is the representation of the 4-hour anneal processes, since the data showed that the time (4-10 hours) was not a significant factor in sheet resistance measurement. The 400°C anneal provided very poor results, indicating that the dopants were not activated at this low temperature. Still, the values show some insight into the process. The highest value is that of the 5E14 Boron implant followed by a 1E15 fluorine implant, meaning that at the time of boron implantation, there was no fluorine or preamorphization present in the wafer. The lowest value is the 5E14F/5E14F implant in which half of the Fluorine was present in the wafer at the time of implant as the three intermediate lines.

At 600°C, the anneals become divided into two distinct segments, one between 5000 and 10,000 ohms/sq, and one near 2000 ohms/sq. These two segments are divided solely on fluorine concentration in the wafer. The higher segment shown is of the 5E14 Fluorine implant (half the amount of the standard BF<sub>2</sub> implants) and that of the exclusively boron implant. The three lines in the lower segment all contain a 5E14 dose of Boron, and a 1E15 dose of fluorine. The order of the implant becomes irrelevant at this process.

At the 800°C anneal, all of the processes result in very similar sheet resistance values, regardless of boron and fluorine concentration. However, the difference in the 600°C anneal is clearly shown by the data.



## REFERENCES

- [1] "International Technology Roadmap for Semiconductors" 2000 Update.
- [2]. Wolf, P. De; Clarysse, T.; Vandervorst, W.; Hellemans, L.; "Low Weight Spreading Resistance Profiling of Ultrashallow Dopant Profiles." Journal of Vacuum Science Technology B. 16(1) Jan/Feb 1998.
- [3]. Clarysse, T.; Vandervorst, W.; "Need to Incorporate the Real Micro-Contact Distribution in Spreading Resistance Correction Schemes."
- Journal of Vacuum Science Technology B.  
18(1) Jan/Feb 2000.
- [4]. Clarysse, T.; Vandervorst, W.; Collart, E.J.H.; Murrell, A.J.; "Electrical Characterization of Ultrashallow Dopant Profiles." Journal of the Electrochemical Society 147(9) 2000.
- [5] P.A. Packan and J.D. Plummer, "Transient Enhanced Diffusion of Low Concentration B in Si due to Si Implantation Damage, Applied Physics Lett., Vol 56, No. 18, p. 1787,1990

# Development of CoSi<sub>2</sub> Salicide Process

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**Abstract** – As RIT is continuously scaling CMOS technology to smaller dimension, the Self-Aligned Silicide (Salicide) process needs to be developed. The silicided metalization leads to low-resistivity gates, interconnections and contacts between the metal and silicon substrate. Currently, salicide processes, such as titanium silicide (TiSi<sub>2</sub>) and cobalt silicide (CoSi<sub>2</sub>), are widely used in advanced CMOS technologies. However, only CoSi<sub>2</sub> salicide process is scalable to deep sub-micron technology, since the resistivity of CoSi<sub>2</sub> phase is independent of the dimensions.

CoSi<sub>2</sub> salicide process using titanium nitride (TiN) as capping film has been developed. Electrical tests were performed: low resistivity of the CoSi<sub>2</sub> and negligible leakage current between gate and source/drain were measured. However, the films showed the presence of cobalt oxide, which might have been incorporated during sputtering step.

## 1. INTRODUCTION

The metal silicides have been a topic of intensive research for more than a decade and have been used extensively in the semiconductor industry. Most of its application is developed for advanced sub-micron CMOS technology to lower sheet resistance (and subsequently RC delay) and to reduce the source/drain parasitic resistance, by forming ohmic contacts in the source/drain regions of MOS transistor, thereby increasing the drive current of the transistors.

The purpose of this work was to develop a self-aligned cobalt silicide process to use for advanced sub-micron CMOS technology in Microelectronic Engineering facility at Rochester Institute of Technology. New applications of CoSi<sub>2</sub>, such as development of high frequency Schottky Junction Transistors [1] and ultra-fast Metal-Semiconductor-Metal photodetector [2], are also possible.

The lines of polysilicon/gate oxide on silicon substrate were used to simulate the MOS gate and drain/source process. Since, the CoSi<sub>2</sub> is independent of line width and doping, it is a reasonable to analyze the self-aligned CoSi<sub>2</sub> formation. In figure 1, the pattern of serpentine structure is shown, which were used to measure resistance of CoSi<sub>2</sub> on top of poly lines:

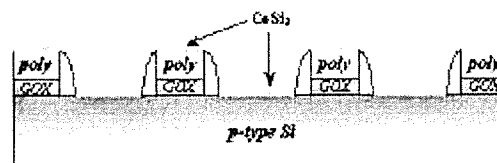


Fig. 1: Cross-section of salicided polysilicon/oxide lines with sidewall spacers to separate poly lines from Si substrate.

## 2. THEORY

### A. Cobalt

The general properties of cobalt (Co) is listed in the table below:

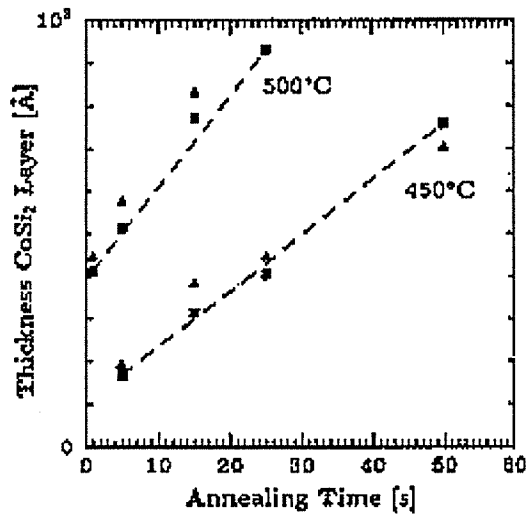
Property	Value	Conditions
Atomic Number	27	NA
Atomic Weight	58.9332	NA
Density	8.9 gm/cc	NA
Melting Point	1495 °C	NA
Boiling Point	2870 °C	NA
Thermal Conductivity	1.00 W/cm/°K	25 °C
Electrical Resistivity	6.24 μΩ·cm	20 °C
Electronegativity	1.8 Paulings	NA

Table 1: General material properties of cobalt

### B. Cobalt Silicide

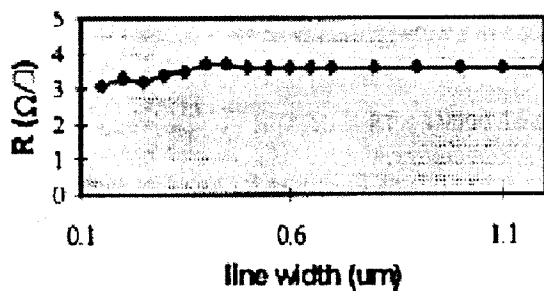
Cobalt silicidation involves the conversion of the complete Co film to the cobalt monosilicide (CoSi) phase during a first rapid thermal annealing and a second conversion to the final CoSi<sub>2</sub> phase during the second rapid thermal annealing. CoSi<sub>2</sub> formation requires an optimal control of the silicidation process and the potential to scale down the process to form thinner layers.

The first anneal of Co plays an important role in the final thickness of the final CoSi<sub>2</sub> film. The reaction is diffusion-controlled and results in layer-by-layer growth [3]. The graph 1 shows the thickness of the CoSi<sub>2</sub> layers resulting from a limited reaction process as a function of the RTP annealing time for 450 °C and 500 °C:

Graph 1: Thickness of CoSi<sub>2</sub> layer vs. anneal time [3]

A selective etch is used to remove the unreacted Co from the SiO<sub>2</sub> regions between two silicidation steps to ensure the self-alignment process. The sheet resistance of CoSi is near or even above 40 Ω/?.

The parameters of a second anneal is not critical. It forms CoSi<sub>2</sub> by forcing Co to diffuse further into silicon, thus making silicon-rich silicide [4]. The sheet resistance of CoSi<sub>2</sub> will not degrade as line width is reduced to sub-quarter micron [5]. This can be seen from the graph below:

Graph 2: CoSi<sub>2</sub> sheet resistance vs. line width

### 3. EXPERIMENTAL

To simulate the gate and source/drain structure of CMOS transistor, the gate oxide layer of 20 nm was thermally grown on p-type silicon wafers and the polysilicon film of 400 nm was deposited, doped with N-250 phosphorous spin-on-glass (SOG) dopant and underwent drive-in step in Bruce Furnace. Next, the SOG dopant was removed by wet etch and polysilicon film was patterned by sub-micron CMOS poly layer mask. After RIE etching patterned polysilicon, the Low Temperature Oxide (LTO) was deposited, densified, and etch-backed to

form sidewall spacers. At that point, wafers were ready for sputtering cobalt and titanium nitride films.

#### A. Cobalt Deposition

Once the CMOS gate structure was simulated, the wafers were ready for sputtering. Patterned and blanket poly wafers were cleaned in H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub> (1:2) solution at 90 °C for 5 minutes to remove any organic and inorganic particles from the surface of the wafers. This was followed by 5-minute rinse and Spin Rinse Dry (SRD). To avoid any native oxide on silicon and polysilicon surfaces, wafers were immersed in hydrofluoric acid (HF) for 20 seconds followed by 5-minute rinse and SRD. This step is critical, since the native oxide is not allowed on the surface where CoSi<sub>2</sub> is forming and at the same time the oxide sidewall spacers are present to separate poly lines and silicon substrate. Therefore, the time should be thoroughly controlled for this step.

The wafers were loaded into CVC 601 sputterer and the base pressure of 7.5×10<sup>-6</sup> Torr was achieved. As discussed later, the base pressure needs to be in low 10<sup>-7</sup> or even mid-10<sup>-8</sup> range to avoid any oxidation of cobalt during sputtering. The condition of sputtering is described in the table below:

Parameters	Conditions
Target Material	Co
Target Size	4"
Pre-heat Time	20 min.
Pre-heat Temperature	300 °C
Base Pressure	7.5×10 <sup>-6</sup> Torr
Gas Flow	58 sccm of Ar
Sputter Pressure	5×10 <sup>-3</sup> Torr
Power	250 Watts
Pre-Sputter Time	5 min.
Sputter Time	5.75 min.
Thickness Deposited	~35 nm

Table 2: Sputtering conditions for cobalt deposition

It should be noted that pre-heating should be done at the beginning of pump-down to evaporate any water molecules from the substrate. Also, the argon (Ar) gas flow might be different in order to achieve the sputter pressure of 5 mTorr.

#### B. Titanium Nitride Deposition

Titanium nitride (TiN) cap is an important step in CoSi<sub>2</sub> formation, since it protects Co from oxidation after the wafers are exposed to atmosphere and during first RTP anneal. It should be done without breaking vacuum. The conditions for TiN sputtering are:

Parameters	Conditions
Target Material	Ti
Target Size	8"
Pre-heat Time	same as for Co dep.
Pre-heat Temperature	same as for Co dep.
Base Pressure	same as for Co dep.
Gas Flow 1	41 sccm of Ar
Gas Flow 2	15 sccm of N <sub>2</sub>
Sputter Pressure	5×10 <sup>-3</sup> Torr
Power	1000 Watts
Pre-Sputter Time	5 min.
Sputter Time	17 min.
Thickness Deposited	~50 nm

Table 3: Sputtering conditions for TiN deposition

TiN film of 30-40 nm might be sufficient to protect Co from oxidation. Also, TiN cap should be stoichiometric with dark orange color. However, the color of TiN depends on the thickness of the film.

### C. First RTP Anneal

The first anneal is performed in AG Associates HeatPulse 410 Rapid Thermal Processor (RTP).

During the first thermal treatment, the deposited Co film is only partially consumed to form an intermediate silicide phase, which is cobalt monosilicide (CoSi). This step is performed at a low temperature. The amount of cobalt consumed for silicidation is completely determined by the temperature and time (see Graph 1). The parameters of first anneal are shown in the table below:

Parameters	Settings
Temperature	520 °C
Time	20-30 sec.

Table 4: Settings for first anneal

Even though, the experimental temperature was set at 520 °C, the setting between 450 °C and 500 °C is desirable. However, RTP was not stable below 520 °C. Also, the time needs to be adjusted in order to make the final CoSi<sub>2</sub> film thicker. Thirty-second anneal resulted in about 10 nm of silicide.

### D. Removal of Co and TiN

After the CoSi was formed at polysilicon lines and silicon substrate, the unreacted cobalt and TiN cap must be removed. It was done by wet etching using sulfuric acid-peroxide solution:

Parameters	Settings
H <sub>2</sub> SO <sub>4</sub> :H <sub>2</sub> O <sub>2</sub>	1:2
Temperature	90 °C
Time	1-2 min.

Table 5: Wet etch parameters and settings

The time might vary to etch off Co and TiN, since the hydrogen peroxide is evaporating, thus changing the proportion of the chemicals. It etches faster for the first wafer. The formed CoSi will not be effected by this etch, so it is not critical if the wafers is overetched.

### E. Second RTP Anneal

The second RTP annealing is the final step of the CoSi<sub>2</sub> formation. However, it needs to be confirmed that CoSi film has been formed. It can be easily done by measuring sheet resistance using four-point probe. The high sheet resistance of around 40 Ω/? was observed for the wafers after the wet etch. The settings for second anneal are:

Parameters	Settings
Temperature	750 °C
Time	30-50 sec.

Table 4: Settings for second anneal

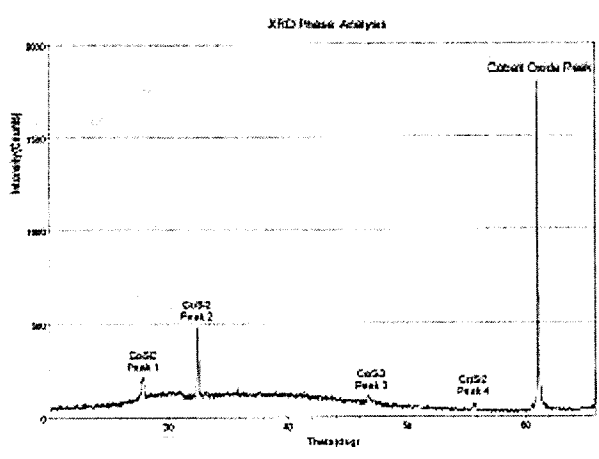
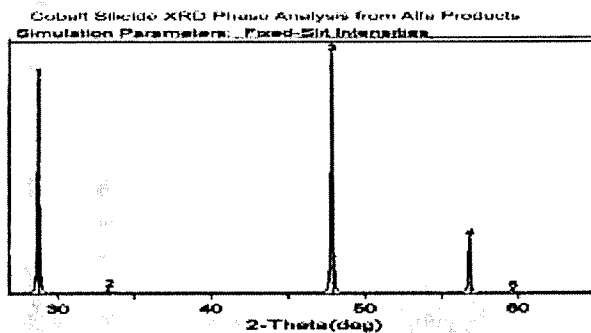
The time was varying from 30-50 seconds, which showed slight improvement in sheet resistance for longer time. It might be due to forming all of CoSi into CoSi<sub>2</sub>. The sheet resistance went down from 40 Ω/? of CoSi to 17 Ω/?.

## 4. DISCUSSION

### A. XRD Analysis

X-Ray Diffraction (XRD) analysis is a certain way to find out the nature of the film. The pattern of a scanned sample of the wafer was compared with the sample of CoSi<sub>2</sub> XRD pattern, which was obtained from Alpha Products. It was noticed that all phase peaks were shifted by one degree from the Alpha Products' pattern. Also, one peak of CoSi<sub>2</sub> was replaced by the cobalt oxide peak, which might have been caused by oxygen incorporation during the sputtering.

The peak shift was probably resulted from the cobalt oxide peak, which slightly changed the structure of the film. XRD pattern in Figure 2 shows the CoSi<sub>2</sub> peak 1 through 4 and peak 5 is cobalt oxide peak. The XRD pattern of CoSi<sub>2</sub> (Figure 3) was obtained from Alpha Products.

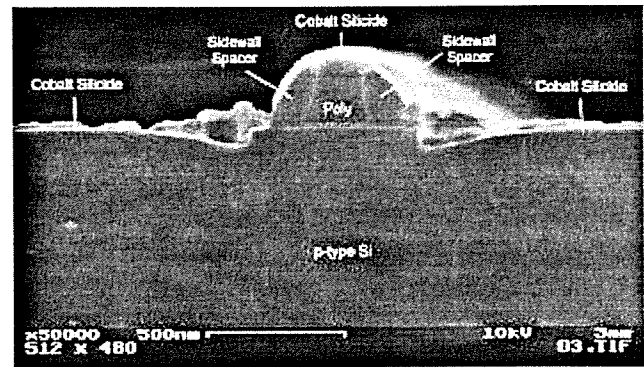
Fig. 2: XRD pattern of CoSi<sub>2</sub> from one of the wafers.Fig. 3: XRD pattern of CoSi<sub>2</sub> from Alpha Products

As it can be seen from figure 2, the cobalt oxide peak at 61 ° is present. Since CVC 601 sputterer does not allow the base pressure go below mid range of  $10^{-6}$  Torr, the oxygen molecules are present in the chamber during Co sputtering. This causes oxidation of cobalt, which is very sensitive to oxygen.

### B. SEM Images

In order to visually see the cross-section of the structure, the Scanning Electron Microscope (SEM) was used. The figure 4 shows the exact structure of the formed line. The sidewall spacers are formed around poly line. The poly line is about 300 nm wide, which is result of isotropic etch in GEC Cell using SF<sub>6</sub> gas, since the patterned lines should be around one micron. Also, from the step height at the bottom of poly line, it can be seen that wafer has been overetched during back-etching of sidewall spacers and dipped into HF solution right before the sputtering step. HF solution etched oxide spacers laterally resulting in step height. Cobalt silicide could be seen on silicon substrate. CoSi<sub>2</sub> conformed a thin film to silicon substrate surface. However, it is harder to see the CoSi<sub>2</sub> on poly line, since the film is very thin (around 10 nm). The grains on the substrate are from the CMP slurry,

which were deposited during polishing the sample before taking SEM image.

Fig. 4: SEM image of CoSi<sub>2</sub> on silicon/poly line. Sidewall spacers prevented CoSi<sub>2</sub> formation during annealing.

Here is another SEM image taken from the top angle. It shows that poly lines were overetched.

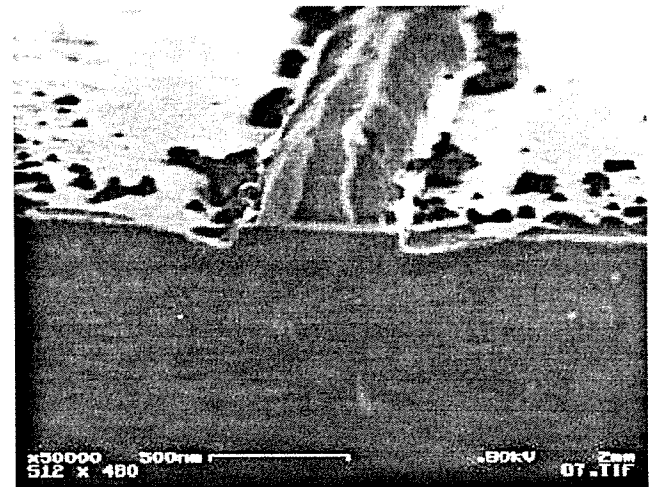
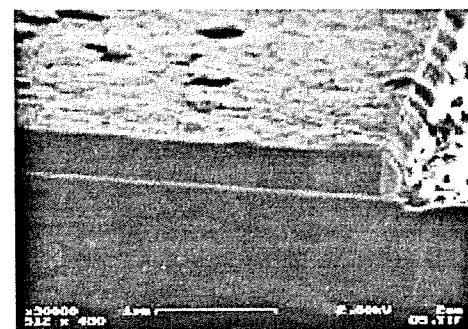


Fig. 5: SEM image of another poly line.

Next image shows the three-micron poly line. The same pattern of sidewall spacers and overetched substrate is observed. It is still hard to see CoSi<sub>2</sub> on the line but it is obvious that the film is conformal.

Fig. 5: SEM image of CoSi<sub>2</sub> on three-micron poly line.

### C. Electrical Test

The tests were performed on HP 4145A Semiconductor Parameter Analyzer to measure the line resistivity and leakage current. The test structures are shown below:

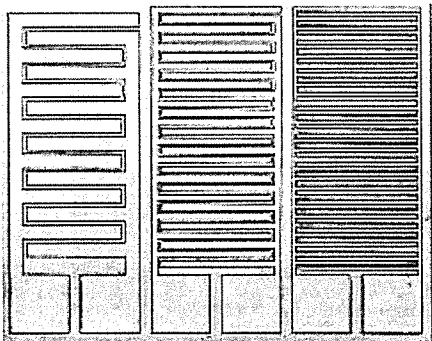


Fig. 6: Comb structures with space separation of 6  $\mu\text{m}$ , 4  $\mu\text{m}$ , and 2  $\mu\text{m}$  (from left to right)

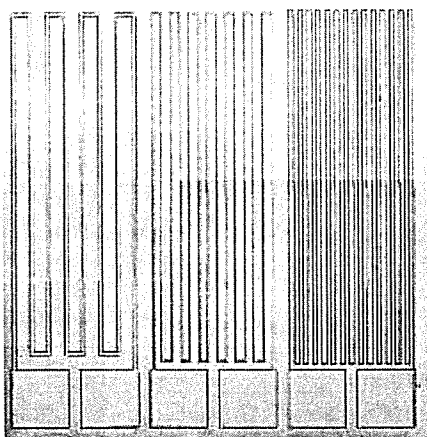


Fig. 7: Serpentine structures with total squares of 890, 2800, and 32000 (from left to right)

The resistance of the comb structures was tested before and after  $\text{CoSi}_2$  formation. The resistance of the comb space separation prior to  $\text{CoSi}_2$  layer has been measured on multimeter and showed an infinite resistance, which is greater than 20  $\text{M}\Omega$ . After the formation of  $\text{CoSi}_2$ , the resistance is shown below:

Separation	V (V)	I (nA)	R ( $\text{M}\Omega$ )
Small (2 $\mu\text{m}$ )	2	36.7	54.5
Medium (4 $\mu\text{m}$ )	2	9.22	217
Large (6 $\mu\text{m}$ )	2	3.15	635

Table 5: Leakage current and resistance between the poly lines of comb structure at 2 V.

The actual separation is not known, however the poly lines underwent an isotropic etch in GEC Cell and got reduced laterally. The resistance and the leakage current

are shown to be reasonable if the area of the lines is taken into consideration.

The resistance of serpentine lines was also measured before and after the formation of  $\text{CoSi}_2$ . The resistance and sheet resistance are shown in Table 6:

Linewidth / Sq.	Before		After	
	R ( $\text{k}\Omega$ )	$R_s$ ( $\Omega/?$ )	R ( $\text{k}\Omega$ )	$R_s$ ( $\Omega/?$ )
Small / 35000	950	27.1	848	24.5
Medium / 2800	82.2	29.4	15.9	5.68
Large / 890	25.8	29.0	4.96	5.57

Table 6: Resistance and sheet resistance of  $\text{CoSi}_2$ /poly serpentine lines before and after  $\text{CoSi}_2$  formation.

The resistance and sheet resistance of small serpentine line are higher than expected. Since isotropic etch of poly lines in GEC Cell distorted the profile of the line, it is not uniform in width and some areas are thinner than others. It also can be seen on SEM image in figure 5.

## 5. CONCLUSION

Overall, the  $\text{CoSi}_2$  salicide process has been demonstrated to be successful. It significantly reduced the resistance of the poly lines and silicon substrate surfaces. Also, it has been proven that the self-aligned process is established with negligible leak current and high resistance between the lines and substrate. XRD analysis confirmed the pattern of  $\text{CoSi}_2$  film.

However, the time for first anneal needs to be increased to make  $\text{CoSi}_2$  film thicker. Also, if RTP is capable, the temperature needs to be decreased to 450-500  $^\circ\text{C}$  for the first anneal step. This will ensure the proper formation of cobalt monosilicide.

Another issue that should be taken into consideration is the cobalt oxide in the  $\text{CoSi}_2$  film. The base pressure in the sputter tool needs to be in the low  $10^{-7}$  or even in the mid- $10^{-8}$  Torr range. This will prevent the oxidation of Co during sputtering.

## REFERENCES

- [1] Trevor J. Thornton, "Schottky Junction Transistor – Micropower Circuits at GHz Frequencies," *IEEE Electron Device Letters*, vol. 22, pp. 38-40, 2001
- [2] S. Mantl, et. al, "Growth, Patterning and Microelectronic Applications of Epitaxial Cobalt Disilicide," *MRS Symp. Proc.*, Volume 514, 1998
- [3] K. Maex and R. Schreutelkamp, "Self-Aligned Silicides for ULSI," *MRS Symp. Proc.*, Volume 260, p. 143, 1992
- [4] S.P. Murarka, "Silicides for VLSI Applications", Academic (1983)

- [5] B. Conaghan, Y. Hu, Y. Xu, "Applications of silicides in semiconductor processing," Univ. of Maryland, <http://www.ece.umd.edu/class/enee697.S99/projects/xyh/enee697-1cover.html>

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# Electrolytic Plating of Copper

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**Abstract--** ReynoldsTech graciously donated a copper-electroplating tool to R.I.T., which speaks volumes and has far reaching potentials and challenges for, innovative research, patents and, incorporation of the damascene process into the thin film labs. Upon eventual integration into the classroom environment further designed experiments, process improvement and senior design projects, electroplating will eventually replace the existing aluminum metal layers with copper for the advanced 1.0 $\mu$ m and 0.5 $\mu$ m CMOS process currently used in the R.I.T. integrated circuit processing student run factory.

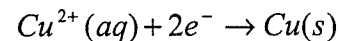
From a ground zero approach with safety issues in mind the ramping up of this new tool had to be installed, a comprehensive manual rewritten, copper sulfate and sulfuric acid electrolyte chemicals added, then characterized and tested to determine its unique capabilities and deposition rates. The experiment used for gathering data incorporated the use of Faraday's Law which states: "the amount of product formed is directly proportional to the charge passed" and "the mass of product formed is proportional to the electrochemical equivalent weight of the product." Following in these footsteps for the theoretical values the ampere-minutes were varied and mass calculated and then compared against the actual mass values by measuring the mass of the wafer before and after plating. An actual thickness was determined and compared against the theoretical values that Faraday calculated.

## 1. INTRODUCTION

With the introduction of the new Copper electroplating tool from ReynoldsTech into the R.I.T. cleanroom facility now a working reality. Integration into the classroom environment will be on the horizon. Students will learn and experiment that copper has a lower resistivity <2m  $\mu$ -cm vs. Aluminum >3m  $\mu$ -cm. Copper also has the following characteristics: a lower sidewall capacitance between adjacent lines, reduced RC time delay which leads to reduced power consumption. Copper also has superior resistance to electromigration, and the lines can be made smaller which equates to a tighter packing density, and the dual damascene process requires 20 – 30% less processing steps.

## 2. BACKGROUND

Much of the early research in electrochemistry was performed by Michael Faraday. It was he who coined the terms anode, cathode, electrode, and electrolyte.<sup>1</sup> In about circa 1833 – 1843, Faraday discovered that the amount of chemical change that occurs during electrolysis is directly proportional to the amount of electrical charge that is passed through an electrolysis cell. The reduction of copper ion at a cathode is given by the equation



The equation tells us that to deposit one mole of metallic copper requires two moles of electrons. The half-reaction for an oxidation or reduction, therefore, relates the amount of chemical substance consumed or produced to the amount of electrons that the electric current must supply.

Following in footsteps of Michael Faraday and his law and Faraday's constant the following relationship can be derived to find the theoretical weight:

$$Mass\ Deposited = \frac{63.546\ g/mol \times (amps \times time)}{2 \times 96,500}$$

Then to relate the mass deposited into a thickness the following relationship was derived

$$Density\ of\ Copper = \frac{Mass\ Deposited}{Volume}$$

$$8.9 \frac{g}{cm^3} = \frac{Mass\ Deposited}{\pi \cdot r^2 \cdot Thickness}$$

$$Thickness = \frac{Mass\ Deposited}{\pi \cdot r^2 \cdot 8.9}$$

where  $r = 4.13\text{cm}$

The only two variables in the above formulas are amperage and time. Those two variables were varied via the plating control terminal (PCT) installed on the electroplating tool. The 100mm wafers were prepared with a sputtered adhesion layer of 1000 angstroms of Tantalum



and Copper seed followed with another 1000 angstroms with excellent adherence. The same was sputtered to 0.7 $\mu$ m trench patterned wafers.

### 3. RESULTS

The preliminary experiments to determine how the tool would react initially revealed bipolar behavior. This phenomenon occurs when the electronic resistance of the seed layer has become smaller than the electrochemical resistance thus under plating the wafer. Evidence of this is when the seed layer at the electrical connection dissolves in and around the exclusion zone, thus creating a bulls-eye effect and under plating the center of the wafer. This was due in part to the electrolytic solution seeping in and behind the wafer and corrupting most of the data when comparing it against theoretical values. A single O-ring was placed behind the wafer to create two seals, one between the stainless steel and copper seed electrical connection and one behind the wafer. This fix steadied the voltage and substantially increased plating thickness bringing the values of theoretical closer to actual with good uniformity.

In the figure 1 below is a plot of sheet resistance as a function of theoretical deposited weight. This plot shows that as the deposited weight is increased the sheet resistance decreases as expected.

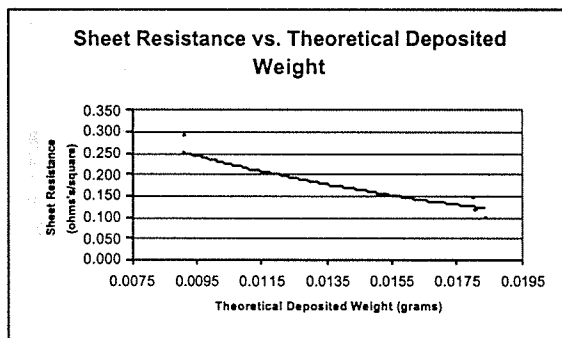


Figure 1

In figure 2 below is a plot comparing the theoretical to actual values for thickness vs. weight. The seven data points are the most recent, and this data represents how the electroplating reacted after the phenomenon of bipolar was concluded and a single O-ring was placed behind the wafer. For both of the graphs the conclusion is the bath concentration needs to be checked and continuously monitored. The bath has not been spiked for ~15 weeks since the volume of electrolytic solution consisting of: 38 liters of CuSO<sub>4</sub>, 26 liters of H<sub>2</sub>SO<sub>4</sub> and 72 Liters of H<sub>2</sub>O was initially added.

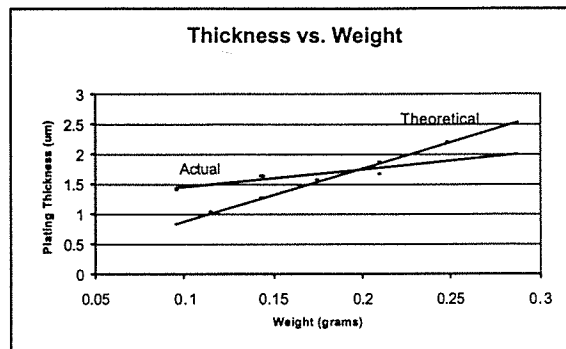


Figure 2

### 4. CONCLUSION

Copper is considered a fast diffuser and can act to "poison" a device in the active area so in taking the necessary logistic steps of isolating copper production a designated wet bench and cautious wafer process handling upgrades to the tool are being carried out. The comprehensive manual incorporates a further look into the various plating screens via the plating control terminal, a get started tutorial was added and a pulse mathematics section to determine and control the plating thickness. Working alone and with extensive tool knowledge a single operator can load the single wafer holder and throughput 6 wafers per hour depending upon the ampere – minutes but dual operator conditions would increase safety margins and shared workloads.

### REFERENCES

- [1] Brady and Holum, "Chemistry, The Study of Matter and Its changes", John Wiley & Sons, NY, p. 768, 1993.

### ACKNOWLEDGMENTS

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**Keith M. Udut**, originally from Lewiston, NY received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2001. He attained co-op work experience at IBM. He is joining IBM as an equipment engineer starting June 2001.

# Carbon Nanotubes: CVD Reactor Design and Growth of Multi-Walled Carbon Nanotubes

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**Abstract--** Carbon Nanotubes are researched to develop for new technology of transporting electrons in one dimension and have commercial potential as nanoscale transistors. Carbon Nanotubes need to be made by using chemical vapor deposition (CVD). This CVD technique is used to deposit thin film on substrates. As the gas decomposes, it frees up carbon atoms, which can recombine in the form of nanotubes. The conditions for the controlled and directed CVD growth of Nanotubes are planned being established with the use of thin film metal catalyst by using RIT's CVD Reactor. This CVD reactor was designed and made for growing the specific, high yield, possibly phase pure, and multi-wall carbon nanotubes in RIT.

## 1. INTRODUCTION

Carbon Nanotube was found by Sumio Iijima, at NEC Fundamental Research Laboratory in Tsukuba, Japan, nearly 10 years ago. Sumio Iijima was studying the material deposited on the cathode during the arc-evaporation synthesis of fullerenes. He found that the central core of graphitic structures including nanoparticles and nanotubes. Carbon nanotubes are fullerene-related structure. These structures consist of graphene cylinders closed at either end with caps containing pentagonal rings, figure 1. Also, the carbon nanotubes are made of pure carbon as regular and symmetric as crystals. These are very tiny tubes about 10,000 times thinner than a human hair.

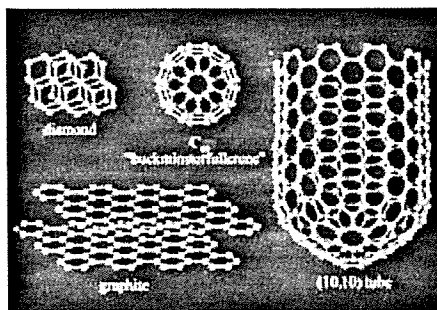


Figure 1: Structure of Carbon Nanotubes

There are two kinds of carbon nanotubes, single- and multi-wall carbon nanotubes. The multi-walled carbon nanotubes, MWCNT, contains a number of hollow cylinders of carbon atoms nested inside one another. This MWCNT was found first by Iijima. Later IBM researchers include Sumio Iijima found single-walled carbon nanotubes, SWCNT. This SWCNT are made of just one layer of carbon atoms.

For the microelectronic industry, these carbon nanotubes are new conduction and insulation materials for devices. The conduction or insulation behavior of carbon nanotubes are depending on how the graphene sheets rolled into a nanotube. The geometry of nanotubes limits electrons to select few slices of graphite's energy state. If they are rolled as straight nanotubes, this makes two thirds of the nanotubes metallic. If they are rolled as twisted nanotubes, the slices of allowed energy state for electrons are similarly cut at an angle, with that results about two thirds of twisted tubes miss the Fermi point and are semiconductors.

Because of the speed, density and efficiency of microelectronic devices all raise rapidly as the minimum feature size decreases, the materials for the devices are getting closed to limit. By many researchers, like IBM, FETs use single semiconduction nanotubes as a channel. Because of its tiny size, the nanotube FET should switch reliably using much less power than a silicon-based device. Theorists predict that a truly nanoscale switch could run at clock speeds of one terahertz of more than 1000 times as fast as processors available today.

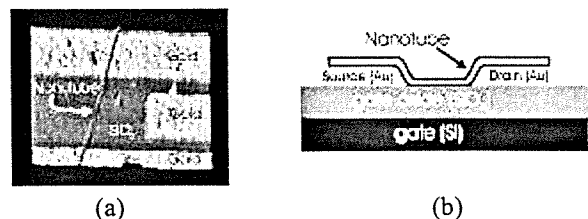


Figure 2: Nanotube Field-effect Transistor from IBM.

(a) actual nanotube FET

(b) closed section of the nanotube FET

There are three ways to grow nanotubes, "zap", "bake" and "blast". In my research, the way of bake, we called chemical vapor deposition (CVD), will be used to grow the nanotubes. This CVD was used to make nanotubes for the first time in Japan. Duke University recently invented a porous catalyst that they claim can convert almost all the carbon in a feed gas to nanotubes. Stan Ford University have been able to control where the tubes from and have been working to combine this controlled growth with standard silicon technology. The growth temperature is typically in the range 500-700°C. At these temperatures the carbon atoms dissolve in the metal nanoparticles that eventually become saturated. The carbon then precipitates to form solid carbon tubes, the diameters of which are determined by the size of the metal particles in the catalyst.

The problem of this project is that we don't have any experience to grow carbon nanotubes at RIT. We don't have any special equipment for only growing carbon nanotubes. Therefore, we are going to make our own CVD equipment for carbon nanotube growing system.

A CVD reactor is a chamber in which gasses at high temperature and controlled pressure undergo chemical reactions that result in growing a thin film on a solid surface (called the substrate) inside the reactor. this CVD reactor can be divided by 3 sections, the gas distribution system, reactor zone, and exhaust system, Figure 3. The major difficulties of CVD research have to do with understanding the complex brew of chemical reactions that occur as the source gasses diffuse toward the substrate. The gasses decompose into fragment molecules, which in turn react with each other and with the unreacted source gas. Some of the fragments stick to the surface, where they recombine to produce a film.

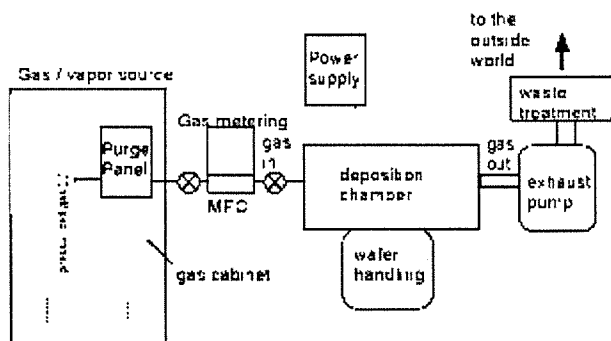


Figure 3: Basic Structure of CVD Reactor

Most Gases and vapors in CVD are for practical purposes "ideal".

$$PV = NRT \quad (1)$$

P is pressure in Pascal, V is volume in m<sup>3</sup>, N is number of moles in gram, R is universal gas constant (=8.3

Joules/mole K), and T is absolute temperature in K. Gas flows are usually measured and reported as standard liters per minute (SLPM) or standard cubic centimeters per minute (SCCM). Both measure gas volume at 0 °C, and 1 atmosphere, these are measures of MOLAR flow. In most CVD applications absolute temperature varies modestly (factors of 2 to 3) whereas pressure varies tremendously large volume expansions occur that is a few cubic centimeters of input gas at atmospheric pressure can become many liters of gas at chamber operating pressure. If we know the geometry, gas flows and composition, and the speed of the reactions at the surface, we can make simple estimates of what is happening inside, using the assumption of a "Zero-dimensional" reactor (simplest non-trivial transport analysis). Concentrations are the same everywhere in the reactor, no gradients.

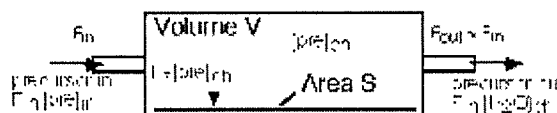


Figure 4: Zero-dimensional theory

From Figure 4, "pre" is precursor chemical for deposition, "[pre]" is concentration (moles/cm<sup>3</sup>, moles/m<sup>3</sup>, moles/liter, as convenient), "F" is volume flow (e.g. m<sup>3</sup>/second), "Ks" is surface reaction rate constant (units of velocity, e.g. cm/second or m/second), "ch" is concentration in chamber, and "in" is inlet concentration. Therefore, the utilization (X) equation can be as equation (2).

$$X = \frac{\text{Moles}(pre)_{in} - \text{Moles}(pre)_{out}}{\text{Moles}(pre)_{in}} \quad (2)$$

When X is approached to zero, it becomes "differential" reactor that concentration is same as inlet concentration. When X is approached to one, it becomes "Starved" reactor that has large gradients in concentration.

Viscous flow equation, equation (3), can be used to calculate effective speed of roughing chamber where the C<sub>1</sub> is volume of chamber and C<sub>2</sub> is the volume of roughing line.

$$\frac{1}{S_{eff}} = \frac{1}{S_p(MP)} + \left( \frac{1}{C_1} + \frac{1}{C_2} \right) \quad (3)$$

Also, the molecular flow equation, equation (4), can be used to calculate effective speed of high-vac pumping

$$\frac{1}{S_{eff}} = \frac{1}{S_p(HVP)} + \left( \frac{1}{C_1} \right) \quad (4)$$

## 2. Chemical Vapor Deposition (CVD) Reactor

By the supports of department of Chemistry and Physics of Rochester Institute of Technology, CVD reactor can be built in the Physics Research Laboratory in the Gosnell Building (RIT building #8). Parts from the used but cleaned and equipments from chemistry department of RIT were used and supported during designing and building CVD reactor.

### A. Design

CVD reactor was designed that followed by some specification, table 1 and figure 5.

Table 1: Specification of CVD reactor

Mechanical Pump Speed		2.2 m <sup>3</sup> /hr
Roughing Chamber	Diameter	1.5"
	Length	35.43"
Roughing Line	Diameter	0.5"
	Length	24"
Gas	Argon	Max 1 l/min
	Methane	Max 1 l/min

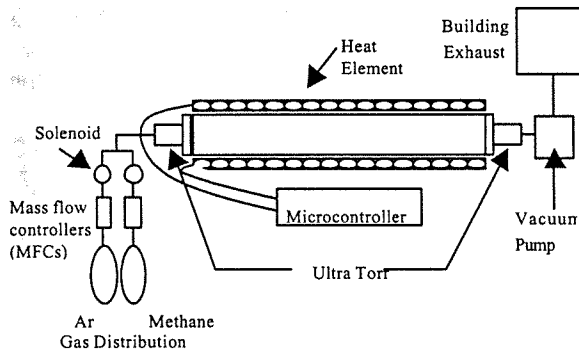


Figure 5: Diagram of CVD Reactor

End caps were designed first. This end caps are called "Ultra Torr", Figure 6, which can make tube easily in vacuum. Also, the tube was designed to fit this end caps.

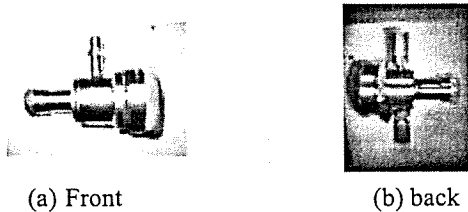


Figure 6: End Caps (Ultra Torr)

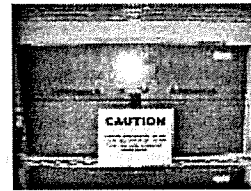
These end caps have 1.5 inches diameter of tube contact and 0.5 inches diameter of input of front and output of back end caps. Therefore, 1.5 inches diameter tube and 0.5 inches line tubes for input and output of gas into the chamber were designed.

The volume of Roughing Chamber can be calculated as equation (5). C1 is the volume of chamber and C2 is the volume of roughing line.

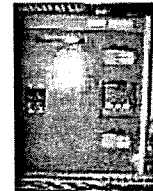
$$C = \pi * \frac{\text{Diameter}^2}{2} * \text{Length} \quad (5)$$

Therefore, C1 is 250.44 in<sup>3</sup>, and C2 is 4.7 in<sup>3</sup>. The effective pumping speed ( $S_{\text{eff}}$ ) can be calculated as equation (3) is 4.3 in<sup>3</sup>/min that is .0043 m<sup>3</sup>/hr.

The chamber tube is located inside of container, Figure 7, that has heater elements and thermocouples. This container was designed to have 3 zones, Load, center, and source. These thermocouples at each zone connected to the microcontroller, Figure 7, that can control the heater of each zone.



(a) Container of heater element



(b) Microcontroller

Figure 7: Heater control equipments

In the gas distribution area, all gases were connected with mass flow controllers (MFC) and solenoids, figure 8. These MFC were designed to control the gas rate in l/min. The purpose of using solenoid is that can protect from back flow from tube and make sure that all unnecessary gases are blocked.

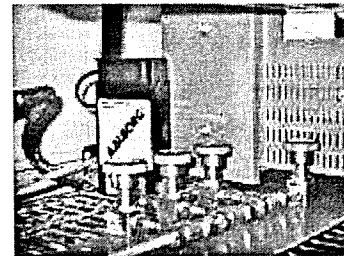


Figure 8: Mass Flow Controller and Solenoids

Due to slow gas pumping was needed, the slow mechanical pump was used, figure 9, with 2.2 m<sup>3</sup>/hr speed. This mechanical pump is dry pump not oil pump because

the methane was used to flow through this pump that can make some hazardous acting with oil.

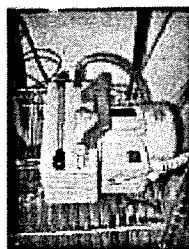


Figure 9: Mechanical Pump

This mechanical pump is connected to the building exhaust system, figure 10. The building Exhaust system is already built in this Lab. Therefore, just connect line from the pump to this system is just needed. This system was designed to exhaust all output gases to outside building.

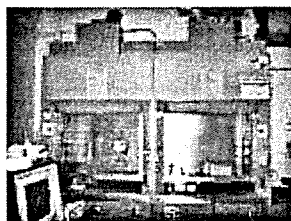


Figure 10: Building Exhaust System

### B. Results and Observation

All equipments were assembled and tested as CVD Reactor for growing nanotubes, figure 11. The actual size of tube was different from design because design was by scale of inches but tube distributors used metrics; therefore, the designed-tube cannot be found. The diameter of actual tube was 3 inches and length of tube was 60.43 inches. The volume of tube is 284.77 cubic inches. The effective speed is change to 17.53 cubic inches per minutes that is four times faster than designed speed, but it is still slow speed that CVD reactor needs.

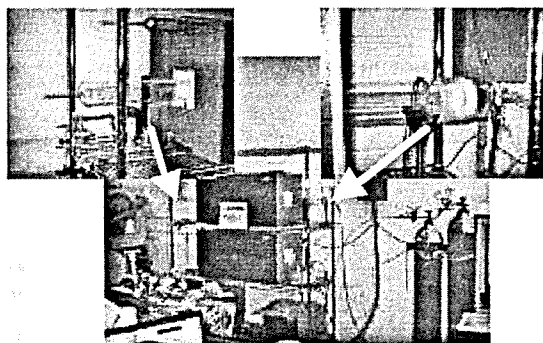


Figure 11: Actual CVD Reactor

The ramping up temperature rate was observed as Figure 11. The rates of ramping up temperature were shown as table 2.

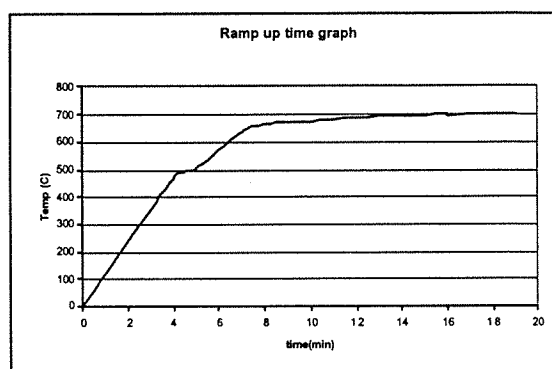


Figure 12: Temperature vs. Time Graph

Table 2: Ramp Up Time Rate Chart

Temperature Range(°C)	Ramp Up Rate(°C/min)
0-500	125
500-650	21
650-700	3.85

Temperature was ramped up very fast as 125 °C per minutes, but it slowed down when temperature reached at 500 °C. For 8 minutes of ramp up time, temperature was already reached to 650 °C; therefore, approximately 10 minutes of ramp up time was needed to reach up to 700 °C.

## 3. GROWING THE SAMPLE OF CARBON NANOTUBES

10 sccm of Methane and 90 sccm of Argon flow at 700°C for 20 min were used for recipe of growing sample of carbon nanotubes. Two runs were performed for this project. At this time multi-Walled Carbon Nanotubes or garphene structure was expected being grown on top of the catalytic film.

### A. Results and Observation

From the first run, there were only catalyst metal, figure 13, that suppose form carbon nanotubes or graphene structure, grew on the silicon. This film was observed as defect from moisture in the lab because these films' adhesion was not well and color was dark gray. The suggestion was using longer dehydrate time without ramp temperature up; therefore, gases were flew for around one hour with out ramping temperature up that may get rid of moisture inside of chamber tube.

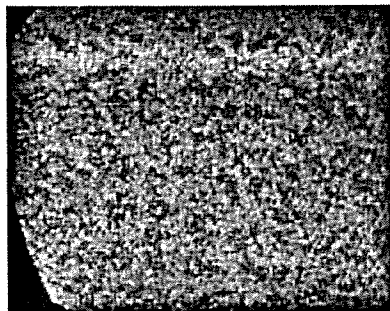
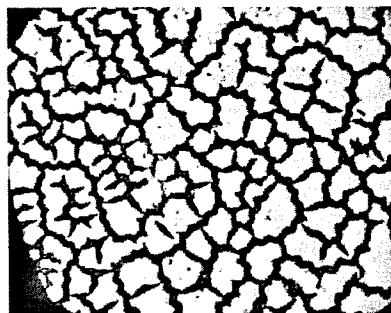


Figure 13: The result film deposition from first run

After second run, the same film as the first run was observed on the top of the silicon, but at the end of the silicon, there were curl structure of catalyst metal were observed. From the microscopic observation, the graphene structure were grew under this catalyst metal, figure 14. From my research, the graphene structure can grow on the catalyst film, but this case showed that if there were gaps between silicon and catalyst film, graphene can grows under the catalyst film.



(a) Curl catalyst film



(b) graphene structure

Figure 14: The result film deposition from second run

#### 4. CONCLUSION

CVD Reactor for growing Carbon Nanotubes was designed and built in RIT. This CVD Reactor was not built as designed because of the chamber tube, but it

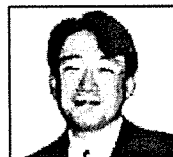
worked and got expected result. This CVD Reactor proved that it could grow carbon nanotubes because it already made graphene structure. But there will be some improvement process needed for forming carbon nanotubes from this graphene structure or catalytic film. In the future, the specific, high yield, possibly phase pure, single and multi-wall carbon Nanotubes can be grown, and nano-electronic devices can be fabricated in RIT.

#### REFERENCES

- [1] P.L. McDuen, H. Dai, W.A. DeHeer, R. Martel, "Carbon nanotubes", *Physics World*, Vol 13, No.6, June 2000, P.29-53
- [2] P. G. Collines, P. Avouris, "Nanotubes for Electronics", *Scientific American*, 2000, P.62-69
- [3] Z. L. Wang, P. Poncharal, W.A. De Heer, "Measuring Physical and Mechanical Properties of Individual Carbon Nanotubes by in situ TEM", *Journal of Physics and Chemistry of Solids*, 61 2000, p. 1025-1030
- [4] C. Journet, P. Bernier, "Production of Carbon Nanotubes", *Applied Physics A materials science & Processing*, A67, 1998, P. 1-9
- [5] S. Arepalli, P. Nikolaev, W. Holmes, C.D. Scoot, "Diagnostics of Laser-Produced Plume under Carbon Nanotube Growth Conditions", *Applied Physics A Materials, Science & Processing*, A 70, 2000, 125-133

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# Ohmic Contact Formation on N-Type 6H-SiC Using Poly-Si and Silicides.

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**Abstract** - Silicon Carbide with its wide bandgap, high thermal conductivity, and high breakdown electric field is an attractive material to be used for applications in high power, and high temperature semiconductor devices. For such applications, it is extremely important to be able to form stable ohmic contacts. Various metals have been attempted to form ohmic contacts on SiC such as Ni, Ti, and Al. However it has been observed that these metallization schemes have degraded performance due to carbon accumulation by forming carbides at the interface. In this study, polycide (poly Si + silicide) based metallizations have been investigated, using  $\text{NiSi}_2$  and  $\text{TiSi}_2$ . Silicides of Ni and Ti have been synthesized employing a layer of heavily doped polysilicon to prevent any form of reaction between the metal and the carbon at the SiC interface. Using a  $0.5\text{cm}^2$  n-type 6H-SiC samples with various doping concentrations ( $1.3 \times 10^{18} \text{cm}^{-3}$  and  $1.7 \times 10^{18} \text{cm}^{-3}$ ), the electrical and structural properties of  $\text{NiSi}_2$  and  $\text{TiSi}_2$  have been examined by fabricating linear transmission line model (TLM) structures. I-V characterization have been carried out to determine the specific contact resistivity,  $\rho_c$ . Samples were processed at various annealing temperatures to determine conditions for the best ohmic contact resistivity.

## 1. INTRODUCTION

For high temperature applications, Silicon Carbide is an attractive material because of the wide band gap (3eV for 6H-SiC) and high thermal conductivity ( $4.5\text{W/K cm}$ ) SiC possesses over Silicon. To fabricate and duplicate the optimum condition for a device, thermodynamically stable ohmic contacts with low specific resistances are required[4]. In most cases, parasitic resistances in the contacts degrade the performance of an electronic device. This paper studies various types of conductive material for contacts, which are processed at different conditions to determine which chemical activity between the metal and the Poly-Si interface would yield the lowest ohmic contact resistivity.

Generally on an n-type substrate, nickel(Ni) would be the preferred choice to form the silicide( $\text{NiSi}_2$ ) by

annealing in a vacuum at  $900^\circ\text{C}$  to  $1100^\circ\text{C}$ . The reaction between the Si in SiC with Ni yields a second substance aside from  $\text{NiSi}_2$ , which is Carbon. There have been studies showing that Carbon hampers the ability to attain low resistance[2]. Therefore this study would look into alternative methods in arriving at low thermally stable ohmic contacts.

One possibility is joining metals such as Ti, and Ni to a deposited layer of doped poly-Si to react and form a silicide without the removal of any carbon from the SiC interface. The added Si thin film layer would arrest the residual Carbon atom in the electrode layer. Samples will be processed at various annealing temperatures to monitor which setting yields the best ohmic contact resistivity,  $\rho_c$ . In general,  $\rho_c$  cannot be measured directly because the current density and voltage distribution under the contact are not consistent. Therefore, the Transmission Line Model (TLM) will be used to indirectly determine the specific ohmic resistivity.

## 2. TLM MEASUREMENTS

The TLM method is based on a simple resistor network to model the ohmic contacts assuming one-dimensional current flow pattern. Three identical contacts are added to the diffused or ion-implanted sheet with contact spacing  $d_1$  and  $d_2$ . The TLM structure consists of test structures of several rectangular contact pads of length  $L$ , and width  $W$ .

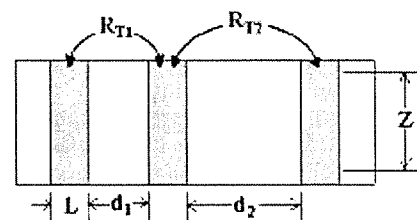


FIG. 1. TLM Structure, showing Schokley pads 1 through 3; dark area is contacts, light area is 6H-SiC.

The total resistance between two contacts in dependence of the different spacings  $d_i$  between the contacts can be described by:

$$R_{Ti} = 2R_C + \frac{R_{SH}d_i}{Z} \quad (1)$$

where  $R_C$  represents the contact resistance and  $R_{SH}$  is the sheet resistance of the semiconductor layer outside the contact region[4]. By solving for  $R_C$ , the ohmic resistance can be calculated by taking the difference between the two pairs of contacts. Similar to solving for two equations and two unknowns, contacts resistance can be written as

$$R_C = \frac{(R_{T2}d_1 - R_{T1}d_2)}{2(d_1 - d_2)} \quad (2)$$

Another critical element for solving the specific contact resistivity is the transfer length,  $L_T$ . The transfer length can be thought of as the length where the voltage due to the current transferring from the semiconductor to the metal or from the metal to the semiconductor has dropped to  $1/e$  of its maximum value. In the case where the contact length ( $L$ ) is greater than or equal to  $1.5L_T$ , specific contact resistivity can be written as

$$\rho_c \approx (L_T)(Z)(R_C) \quad (3)$$

The value of  $\rho_c$  was calculated from equation 3.0. The value of  $L_T$  is half of  $d$  at  $R_T=0$ [4]. The value of  $R_C$  is half of  $R_T$  at  $d=0$ [4].

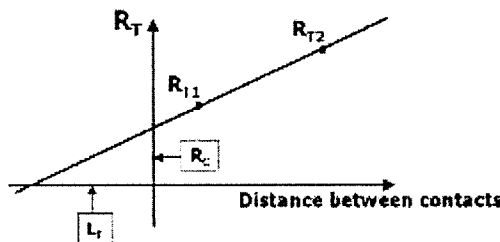


FIG. 2. Theoretical representation of  $R_T$  vs.  $d$  measurement for each pad spacing.

Essentially TLM modeling can be looked at as a three terminal contact resistance method. By moving away from two terminal structures, TLM modeling removes the ambiguity that existed with the two terminal method by not including the bulk resistance and the layer sheet resistance from the specific contact resistivity calculation. TLM modeling also incorporates the transfer length to consider the effect of current crowding on specific contact resistivity. However, specific resistivity values measured with the TLM model may be subject to systematic error due to the TLM is based on a simplified model of the metal-semiconductor contact[4]. The model assumes identical contact resistances for all three or more contacts, which is questionable but reasonable for a sample that is

not too large. In addition, the contact resistance is obtained by taking the difference of two large numbers, which introduces significant error, especially in the case when the contact resistance is very low. To reduce the amount of error, and increase the amount of confidence in the result, multiple measurements of  $R_T$  is obtained to determine  $\rho_c$ .

### 3. EXPERIMENTAL

The devices were fabricated entirely at the RIT facility starting from bare SiC to operating TLM structures. The substrate used in this project were (0001)-oriented p-type 6H-SiC substrate, which were provided by Cree Research Inc., consisting of a  $4\mu\text{m}$  thick nitrogen doped n-type ( $1.3 \times 10^{18} / \text{cm}^3$  and  $1.7 \times 10^{18} / \text{cm}^3$ ) epitaxial layer. The goal was to process a TLM contact structure using  $\text{TiSi}_2$ , and  $\text{NiSi}_2$  on both types of net doping concentrations. The TLM contact structures were spaced apart unevenly ( $d=15\mu\text{m}$ ,  $25\mu\text{m}$ ,  $45\mu\text{m}$ ,  $85\mu\text{m}$ ,  $170\mu\text{m}$ , and  $335\mu\text{m}$ ) with a line widths of  $60\mu\text{m}$ . As a prelude to this project, one more sample was processed with  $\text{TiSi}_2$ , to observe the change in specific ohmic contact resistivity at a different annealing temperature.

#### A. Poly-Si

After running all the samples through a standard RCA clean (HPM + APM), approximately 400nm of poly-Si was deposited using LPCVD with  $\text{SiH}_4$  as a reactive agent. The poly-Si is then doped with N250 Phosphorous spin on dopant and diffused in  $\text{N}_2$  at an annealing temperature of  $1000^\circ\text{C}$  for 15min. soak drive-in.

#### B. Nickel Silicide ( $\text{NiSi}_2$ )

One sample from each dopant concentration was set aside for  $\text{NiSi}_2$  contacts. An RF-sputter-system (base pressure  $8 \times 10^{-6}$  Pa) equipped with a 4" Ni compound target was used to deposit 95nm of Ni onto the samples. The thickness of Ni and Poly-Si were calculated so that after an annealing process, the thin films would form a stoichiometric  $\text{NiSi}_2$  alloy, assuming that the density of the deposited material is identical to that of the bulk[1]. A first level lithography step was performed to create the lines for the TLM structures, which acts as a masking layer for metal etch and poly-Si etch. The Ni is etched isotropically in a wet etch solution. The poly-Si is anisotropically dry etched with 85% anisotropy, using the DRYTEK QUAD. To isolate the TLM structures into individual n-type wells, an ISOMET low speed saw was utilized to cut  $10\mu\text{m}$  into the 6H-SiC substrate, assuring to cut well past the underlying epilayers. The samples were annealed at  $950^\circ\text{C}$  for 1min. in Ar flow. The annealing of the samples were carried out using a HEATPULSE 410 RTP oven with a quartz base to support the samples. The



composition of the formed alloy was investigated using X-ray Diffraction (XRD) analysis. The HP 4144 analyzer was used to measure the specific ohmic contact resistivity within each TLM contact structures.

### C. Titanium Silicide ( $\text{TiSi}_2$ )

One sample from  $1.3 \times 10^{18} / \text{cm}^3$  dopant concentration and two from  $1.7 \times 10^{18} / \text{cm}^3$  dopant concentration was set aside for  $\text{TiSi}_2$  contacts. An RF-sputter-system (base pressure  $7 \times 10^{-6}$  Pa) equipped with a 4" Ti compound target was used to deposit 175nm of Ti onto the samples. The thickness of Ti and Poly-Si were calculated so that after an annealing process, the thin films would form a stoichiometric  $\text{TiSi}_2$  alloy, assuming that the density of the deposited material is identical to that of the bulk[1]. A first level lithography step was performed to create the lines for the TLM structures, which acts as a masking layer for metal etch and poly-Si etch. The Ti is etched isotropically in a wet etch solution. The poly-Si is anisotropically dry etched with 85% anisotropy, using the DRYTEK QUAD. To isolate the TLM structures into individual n-type wells, an ISOMET low speed saw was utilized to cut  $10\mu\text{m}$  into the 6H-SiC substrate, assuring to cut well past the underlying epilayers. One sample from each dopant concentration was annealed at  $1000^\circ\text{C}$  for 90s in Ar flow. The additional sample that was processed to observe the change in specific ohmic contact resistivity at a different annealing temperature, was annealed at  $1150^\circ\text{C}$  for 90s in Ar flow. The annealing of the samples were carried out using a HEATPULSE 410 RTP oven with a quartz base to support the samples. The composition of the formed alloy was investigated using X-ray Diffraction (XRD) analysis. The HP 4144 analyzer was used to measure the specific ohmic contact resistivity within each TLM contact structures.

## 4. ANTICIPATED RESULTS

- ◆ *Silicide contact to be preferred over single metal contact*  
Having the poly silicon layer adjacent to SiC would restrict the accumulation of carbon atoms at the interface and in the contact layer. The intentional deposition of poly-Si would change the character of the diffusion process, leading to better ohmic contacts.
- ◆ *Increasing the temperature on the RTA will improve the specific ohmic contact resistivity*  
Annealing at high temperatures would reduce the voltage necessary to have current flow through the contacts. The contacts would form linear IV characteristics.
- ◆ *Certain metals will exhibit better characteristics for resistivity in contact*

When sputtering/annealing metals to form a silicide, thin film resistivity depends on the metals position (Orthogonal, Hexagonal, Tetragonal, and Cubic). Titanium would exhibit a large variation, from  $20 \mu\Omega\text{-cm}$  to  $120+ \mu\Omega\text{-cm}$ . On the other hand Ni is a very stable thin film but is subject to thermal grooving when the silicide develops small individual pockets, which leads to an increase in the electrical resistance. Depending on how the wafers are processed, it would be hard to determine which metal would favor a low ohmic resistivity.

## 5. RESULTS AND DISCUSSION

### A. Electrical characterization

Before processing the samples through an RTP step to form a silicide, the contact resistivity measurements with no heat treatment was recorded.  $1.7 \times 10^{18} / \text{cm}^2$  n-type dopant concentration yielded a specific contact resistivity of  $5.4 \times 10^{-5} \Omega\text{-cm}^2$  and  $5.8 \times 10^{-5} \Omega\text{-cm}^2$  for the poly-Si contact resistivity.  $1.3 \times 10^{18} / \text{cm}^2$  n-type dopant concentration yielded a specific ohmic contact resistivity of  $4.12 \times 10^{-5} \Omega\text{-cm}^2$ .

The effect of temperature on the  $\text{TiSi}_2$  contacts during the RTP process is illustrated in the figure below.

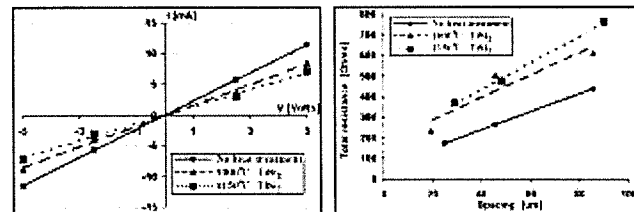


FIG. 3. (a) I-V characterization for  $\text{TiSi}_2$  samples annealed at  $1000^\circ\text{C}$  and  $1150^\circ\text{C}$  for 90s respectively. (b) Total resistance vs. Distance between each contacts on TLM.

The results did not correlate to the expected relationship annealing temperature may have on ohmic resistivity. It is widely understood that by annealing the contacts, specific contact resistivity for  $\text{TiSi}_2$  is expected to improve. There was a rise in total resistance, when the temperature was altered from  $1000^\circ\text{C}$  to  $1150^\circ\text{C}$ . This increase in resistance can be attributed to the oxidation that must have taken place from the time the titanium was sputtered, to the moment the contacts were ready for anneal. If this were the case, by annealing an oxidized film, there is a possibility of forming a parasitic contact in place of an ohmic contact. This parasitic contact layer would inhibit the current from flowing through the contacts, which would increase the amount of voltage required to obtain a measurement. Ohms law states under these conditions, the total resistance would increase

linearly. Despite the increase in total resistance, measurements performed on  $1.7 \times 10^{18} / \text{cm}^2$  dopant concentration for specific contact resistivity showed an improvement in value as the annealing temperature was increased. A  $1000^\circ\text{C}$  anneal for  $\text{TiSi}_2$  provided a specific contact resistivity value of  $9.858 \times 10^{-4} \Omega\text{-cm}^2$ . A  $1150^\circ\text{C}$  anneal for  $\text{TiSi}_2$  provided a specific contact resistivity value of  $6.678 \times 10^{-4} \Omega\text{-cm}^2$ . Unfortunately measurements for  $1.3 \times 10^{18} / \text{cm}^2$  dopant concentration was not obtained.

For  $\text{NiSi}_2$ , measurements performed on  $1.3 \times 10^{18} / \text{cm}^2$  dopant concentration yielded a specific contact resistivity value of  $4.058 \times 10^{-3} \Omega\text{-cm}^2$ . Once again, the increase in specific resistivity from no heat treatment to  $950^\circ\text{C}$  anneal for  $\text{NiSi}_2$  can be attributed to the oxidation that must have taken place from the time the nickel was sputtered, to the moment the contacts were ready for anneal. Unfortunately measurements for  $1.7 \times 10^{18} / \text{cm}^2$  dopant concentration was also not obtained.

### B. Thin film analysis

XRD has been used to examine the reaction within the polycide film by determining the metal position of the particular silicide formed. The composition for  $\text{TiSi}_2$  was determined to be orthogonal, and the composition for  $\text{NiSi}_2$  was determined to be cubic.

XSEM was employed to determine the rate and amount of consumption for poly-Si during RTP. This chart below serves as a guide to anticipate how thick each film stack should be to process the desired amount of silicide, and the desired amount of poly-Si left behind after an RTP step.

Amount of Silicon Required to Form Silicide				
Metal	Atomic Volume [ $\text{\AA}^3$ ]	Silicide	$\text{\AA}$ of silicon Per $\text{\AA}$ of metal	$\text{\AA}$ of Resulting Silicide thickness per $\text{\AA}$ of metal
Ti	10.60	$\text{TiSi}_2$	2.27	2.51
Ni	6.60	$\text{NiSi}_2$	3.65	3.63

TABLE 1. A conversion table to calculate optimal remaining poly-Si thickness and silicide thickness after an RTP step.

For Instance, if 100nm of titanium is reacted with poly-Si to form  $\text{TiSi}_2$ , a minimum of 227nm of poly-Si is required. In addition, the 100nm of titanium would result in a  $\text{TiSi}_2$  thickness of 251nm.

Two samples with similar doped poly-Si thickness and titanium thickness were processed to demonstrate and produce a difference in consumption rate for poly-Si. The annealing temperature to form  $\text{TiSi}_2$  was altered for both samples. One sample underwent an RTP processing step of  $850^\circ\text{C}$ , while the other sample was processed at  $1300^\circ\text{C}$ .

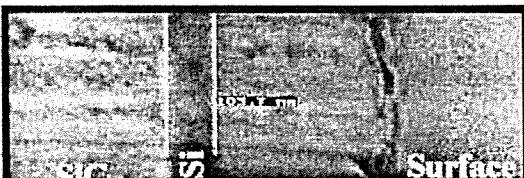


FIG. 4.  $\text{TiSi}_2$  for  $850^\circ\text{C}$  RTP anneal.

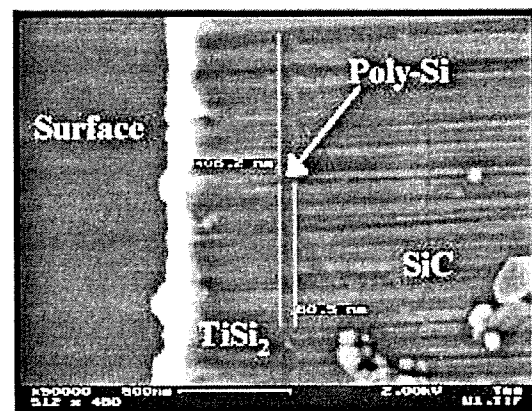
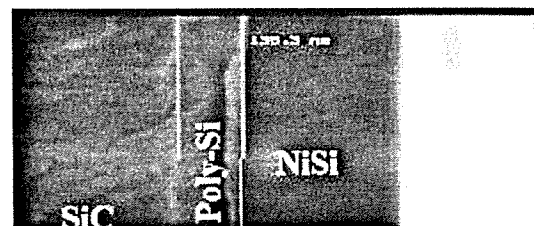


FIG. 5.  $\text{TiSi}_2$  for  $1300^\circ\text{C}$  RTP anneal.

The results indicate a large amount of poly-Si reacted with the refractory metal to form  $\text{TiSi}_2$  at elevated temperatures. Using the values in Table 1, assuming all of the poly-Si is reacted with the metal, the expected  $\text{TiSi}_2$  thickness is  $4910\text{\AA}$ . The anneal of  $850^\circ\text{C}$  resulted in a  $\text{TiSi}_2$  thickness of  $3565\text{\AA}$ , which is shy of the targeting thickness. This is attributed to the remaining poly-Si of  $1037\text{\AA}$  that went unreacted. On the other hand the anneal of  $1300^\circ\text{C}$  resulted in a  $\text{TiSi}_2$  thickness of  $4062\text{\AA}$ , which is also shy of the targeting thickness, due to a smaller amount of poly-Si that did not react with the refractory metal.

In the case of nickel silicide, two more samples with similar doped poly-Si thickness and nickel thickness were processed to demonstrate and illustrate the consumption rate of poly-Si is in fact a function of annealing temperature. The annealing temperature to form  $\text{NiSi}_2$  was altered for both samples. One sample underwent an RTP processing step of  $850^\circ\text{C}$ , while the other sample was processed at  $950^\circ\text{C}$ .



RTP temperature was raised from 1000°C to 1150 °C. In addition, an age test at 545°C for 50h showed significant improvement in specific contact resistivity and sheet resistance for both types of silicides.

## REFERENCES

- [1] Ohmic contact formation on n-type 6H-SiC using NiSi<sub>2</sub>, Nakamura, Tomonori; Shimada, Hisanori; Satoh, Masataka, Materials Science Forum, v338 (II), 2000 Trans Tech Publ Ltd, Uetikon-Zuerich, Switzerland, p 985-988
- [2] Characterization of ohmic and Schottky contacts on SiC, Kakanakova-Georgieva, A.; Marinova, Ts.; Noblanc, O.; Arnodo, C.; Cassette, S.; Brylinski, C., Thin Solid Films, v 343, 1999 Elsevier Sequoia SA, Lausanne, Switzerland, p 637-641
- [3] Improved ohmic contact on n-type 4H-SiC, Gao, Y.; Tang, Y.; Hoshi, M.; Chow, T.P., Solid-State Electronics, v44, n10, Oct, 2000 Elsevier Science Ltd, Exeter, Engl, p 1875-1878
- [4] Characterization of sputtered titanium silicide ohmic contacts on n-type 6H-silicon carbide, Getto, R.; Freytag, J.; Kopnarski, M.; Oechsner, H., Materials Science and Engineering B: Solid-State Materials for Advanced Technology, v 61, 1999 Elsevier Sequoia SA, Lausanne, Switzerland, p 270-274
- [5] Low specific resistance TiC ohmic contacts to n-type  $\beta$ -SiC, J.D. Parsons, G.B. Kruaval, A.K. Chaddha, Appl. Phys. Lett, v 65, 1994, p 2075-2077

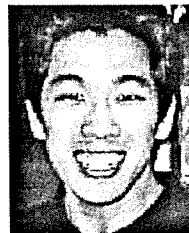
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2001.

Asuka Nomura, originally from Los Angeles, CA, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2000. He attained co-op work experience at Advanced Micro Devices for a year and a half. He is joining AMD Corporation as a Process Development Engineer starting August

FIG. 6. NiSi<sub>2</sub> for 850°C RTP anneal.

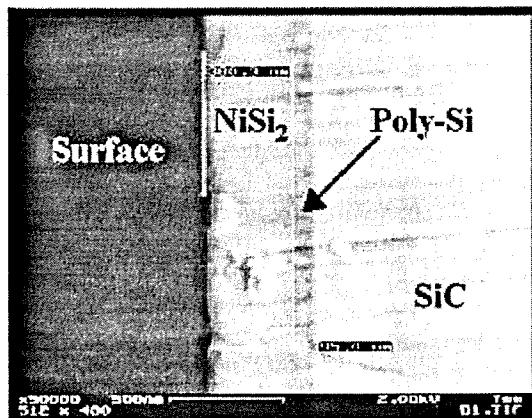


FIG. 7. NiSi<sub>2</sub> for 950°C RTP anneal.

The results indicate a large amount of poly-Si reacted with the refractory metal to form NiSi<sub>2</sub> at elevated temperatures. Using the values in Table 1, assuming all of the poly-Si is reacted with the metal, the expected NiSi<sub>2</sub> thickness was 3993Å. The anneal of 850°C resulted in a NiSi<sub>2</sub> thickness of 3457Å, which is shy of the targeting thickness. This is attributed to the remaining poly-Si of 1383Å that went unreacted. On the other hand the anneal of 950°C resulted in a NiSi<sub>2</sub> thickness of 3803Å, which is also shy of the targeting thickness, due to a smaller amount of poly-Si that did not react with the refractory metal.

## 6. Conclusions

The average poly-Si specific contact resistivity measured on  $1.7 \times 10^{18} \text{ cm}^{-3}$  net doping concentration was approximately  $5 \times 10^{-5} \Omega\text{-cm}^2$ . As silicides were formed onto the TLM structure, the increase in specific contact resistivity can be attributed to the oxidation that must have taken place from the time the metal was sputtered, to the moment the contacts were ready for anneal. Perhaps a metal capping layer is necessary before silicidation to avoid forming a parasitic layer on the TLM structures. Despite the increase in resistance, a drop in resistance was observed when the

# Fabrication and Characterization of 6H-SiC Photovoltaic Devices

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**Abstract--** Silicon Carbide (SiC) photovoltaic (PV) devices have caught the interest for extra terrestrial endeavors. This is due to the excellent resistance to radiation, good thermal conductivity, and high quantum efficiency of such devices. Also the large band gap (of 2.9eV) makes it ideal for gathering high-energy UV photons thus creating a large power density.

Using 1cm<sup>2</sup> 6H-SiC diode samples, photovoltaic cells were produced. Both P-on-N and N-on-P were examined for this study. There are two samples for each type with varying doping concentrations. For the n-side of each sample, a multilayer of Ti/Ni/Al metals was deposited to have ohmic contact to the substrate. For the p-side, Al metal was deposited. A spectral response will be studied on these devices in the 200-400nm range and quantum efficiency will be determined for an AM0 (atmosphere in space) spectral output. The devices will also be tested over a range of temperatures to see how efficiency changes. Other responses that will be characterized are maximum power output, fill factor, built-in forward bias voltage, breakdown voltage, and the dark leakage current. Combining all of the above responses will help in optimizing photovoltaic devices to best serve the needs of power and efficiency.

## 1. INTRODUCTION

Silicon Carbide (SiC) has caught the interest of using photovoltaic (PV) devices for extraterrestrial endeavors. This is due to the excellent resistance to radiation and good thermal conductivity of such devices. Also the large band gap (of 2.9eV) makes it ideal for gathering high-energy UV photons. Along with high quantum efficiency, a large power density is created.

SiC is an excellent choice due to high radiation resistance. This is very important factor when dealing with extraterrestrial applications since there is no protection from undesired radiation in space that could damage the devices.

Since there is no protection from radiation, there is radiation through the full electromagnetic spectrum. SiC photovoltaic devices have a high quantum efficiency (that

is producing the electricity from the amount of radiation impinged upon the device) in the UV range of 200-400nm. Utilizing the large 2.9eV band-gap of SiC, high-energy UV radiation can be gathered by the SiC photovoltaic device to produce a large power output from devices.

However the lower energy radiation (such as visible and infrared) may cause heat in the device since they are not energetic enough to produce electricity across the diode. Also the heat generated from the sun will also heat the device. As photovoltaic devices heat up, they tend not to be quite as efficient. Good thermal conductivity is essential, especially in space, to help reduce the effect of heat on a device. SiC devices show good thermal conductivity.

For this study, 1 cm<sup>2</sup> SiC samples were used with various doping concentrations and different device type (P-on-N or N-on-P). Using these devices, the I-V characteristics will be studied. This will produce a good knowledge base and further studies on how to optimize SiC photovoltaic devices.

## 2. EXPERIMENTAL PROCEDURE

Four existing 1cm<sup>2</sup> doped 6-H SiC samples were obtained. The characteristics of these cells are as follows in Table 1. A quartz mask was designed and made for the imaging of a top contact for the photovoltaic devices.

Table 1: Cell Characteristics for study

Sample #	1	2	3	4
Type	P-on-N	P-on-N	N-on-P	N-on-P
Bottom Doping (cm <sup>-3</sup> )	3.5E+17	3.0E+17	8.0E+17	6.5E+17
Top Doping (cm <sup>-3</sup> )	2.1E+18	3.0E+18	1.3E+18	1.7E+18
Junction Depth (um)	0.4	0.4	0.4	0.4

(1)

### A. Processing

Samples were first adhered to 4" silicon wafers with the N-side up. For creating contacts on the N-side, a CVC 601 sputtering tool was used to deposit a Ti/Ni/Al contact with the thicknesses at 200Å/750Å/100Å. When annealed the nickel will start to form a silicide with the SiC substrate. However, this would leave a build up of carbon at the interface, which would create high resistance at the interface. By having the titanium, it combines with the carbon to create TiC and reduces the interface contact resistance. The aluminum is used as a capping layer so an oxide is avoided when annealing.

The samples are then removed from the wafers, cleaned, and adhered back onto the silicon wafers, this time with the P-side up. Using the CVC601 Sputter tool again, a 1000Å Al metal contact was sputtered.

Next, the N-on-P samples were removed from the silicon wafers turned around to the top side of the device and adhered back on to the silicon wafers. A photolithography step was done to create an image in resist for the top contact.

For the N-on-P samples, etching was done. Using aluminum etch the Al and Ni layers were etched. Next the Ti was etched using diluted HF (HF/Water 1:50). Once the etches were done, the line width of the contacts were measured to make sure they were the right length. For the P-on-N samples, etching was done by using aluminum etch to the Al.

The next thing to do was to anneal the wafers to create a better contact between the substrate and the metal contacts. After this the samples were ready to be tested.

### B. Testing

First, an AM0 flood exposure is done to obtain an I-V curve. From the I-V curve the open circuit voltage, short circuit current, and maximum power output can be measured. Fill factor can be calculated as follows.

$$(1) \quad FF = \frac{P_{\max}}{V_{OC} * I_{SC}}$$

Next without any exposure, an I-V curve will be generated to determine the dark leakage current.

Also, a spectral response will be measured. This will show what the quantum efficiency is over discrete wavelengths. The quantum efficiency,  $\eta$ , will be calculated as follows.

$$(2) \quad \eta = \frac{P_{\text{output}}}{P_{\text{input}}}$$

Looking over all of these factors per sample the best sample will be determined by which has highest quantum efficiency, highest power output, and largest fill factor.

## 3. RESULTS

Results are yet to be determined. This paper will be revised once results are produced.

## REFERENCES

- [1] D.M. Brown, E.T. Downey, M. Ghezzi, J.W. Kretchmer, R.J. Saia, Y.S. Liu, J.A. Edmond, G. Gati, J.M. Pimbley, W.E. Schneider, "Silicon Carbide UV Photodiodes," IEEE Transaction on Electron Devices, Vol. 40, No. 2, pp. 325-331, 1993.
- [2] F.J. Seiferth, Dr. S. Kurinec, Dr. R. Lane, "Silicon Carbide - The Hot One," 1993
- [3] R.P. Raffaele, S.G. Bailey, P. Neudeck, D. Scheiman, P. Jenkins, S. Hubbard, "Optical and Electrical Characterization of SiC Devices,"
- [4] J.A. McDonald, "SiC Developers on the Cutting Edge," III-Vs Review, Vol. 7, No. 1, pp. 37-40, 1994
- [5] M. Ruff, H. Mitlenher, R. Helbig, "SiC Devices: Physics and Numerical Simulation," IEEE Transaction on Electron Devices, Vol. 41, No. 6, pp. 1040-1054, June 1994
- [6] M.I. Chaundry, W.B. Berry, M.V. Zeller, "Ohmic Contacts on b-SiC," Materials Research Society Symposium Process, Vol. 162, pp. 507-512, 1990
- [7] P. Shenoy, A. Moki, B.J. Baliga, D. Alok, K. Wongchotigul, M. Spencer, "Vertical Schottky Barrier Diodes on 3C-SiC Grown on Si," IEDM94, pp. 411-414, 1994
- [8] Y. Gao, Y. Tang, M. Hoshi, T.P. Chow, "Improved Ohmic Contact on N-type 4H-SiC," Solid-State Electronics, pp. 1875-1878, 2000

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# Design and Fabrication of On-Chip Inductors

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**Abstract--** An inductor is a conductor arranged in an appropriate shape (such as a conducting wire wound as a coil) to supply a certain amount of self-inductance. This passive device stores magnetic energy.

Simple spiral planar inductors of varying geometry were designed and fabricated on a silicon substrate insulated by silicon oxide. The process chosen for fabrication of the devices was the copper damascene process. Line widths and spaces varied from 5 $\mu$ m to 20 $\mu$ m. Thickness of the copper wire was approximately 1.5 $\mu$ m. The inductors were isolated from the silicon substrate by 0.5 $\mu$ m of SiO<sub>2</sub> and wires were insulated with the same material. Theoretical inductance values for the designed inductors ranged from 17nH to 300nH.

## 1. INTRODUCTION

An inductor is a conductor arranged in an appropriate shape (such as a conducting wire wound as a coil) to supply a certain amount of self-inductance [1]. Inductance of two magnetically coupled loops is defined as:

$$L = \frac{\Lambda}{I_1}$$

$\Lambda$  is the flux linkage and  $I_1$  is the current flowing through the loop. Inductance can also be defined as:

$$\phi = \oint B \cdot ds$$

$$L = \frac{\oint B \cdot ds}{I} \text{ (Henry)}$$

Where  $\phi$  is defined as the flux,  $I$  is current, and  $B$  is magnetic flux density. Two example of simple devices that can be modeled are a solenoid and toroidal. The inductance of a simple solenoid device is  $L_{\text{SOLENOID}} = \mu_0 \mu_r n^2 A$  [H]. The inductance of a toroidal device is

$L_{\text{TOROIDAL}} = (\mu_0 \mu_r n^2 h / 2\pi) * (\ln b/a)$  [H], where  $a$  = inner radius,  $b$  = outer radius, and  $h$  = height. It is also important to define the voltage and quality factor ( $Q$ ) of an inductor.

$$V_L = L \frac{dI}{dt}$$

$$Q = 2\pi \frac{\text{Time average energy stored at a resonance frequency}}{\text{Energy dissipated in one period of this frequency}}$$

This passive device allows magnetic energy to be stored, which has many applications in circuit design.

Some applications for inductors on a chip include RF circuits, communications, passive components in microwave circuits, micropower converters, magnetic microsensors, magnetic microactuators, and magnetic MEMS systems. There are several types of inductors that have been fabricated over the years. They can be broken down into three categories; planar types, 3D micromachined planar types, and micromachined planar inductive components with closed magnetic circuits. These groups can be further divided into subcategories. They include spiral, meander, solenoid, and toroidal meander.

Requirements for an inductor on a chip (IOC):

- Must have High current carrying capacity
- High magnetic flux density
- Closed magnetic circuits
- Low product cost
- CMOS compatibility

Areas that require improvement are accurate inductance with small device area, high quality ( $Q$ -) factor, high peak - $Q$  frequency, large inductance ( $L$ ), reduction of substrate loss and metal resistance, minimize both parasitic coupling to the substrate and inductor area, and CMOS

compatibility of process. There are several different methods of reducing substrate loss. These methods include using high resistivity substrate, etching the substrate underneath, insulating the inductor from substrate with thick polyimide, or oxidized porous Silicon (OPS), or diffused shield under oxide (DUO). Ways to reduce metal resistance are thick gold metalization layer, multiple metal layers in parallel, or copper metalization.

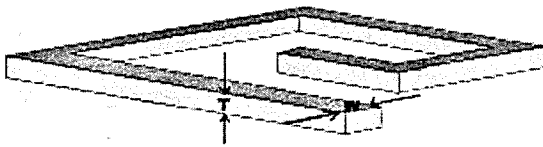
Some of the current inductor technologies are two level planar inductor using normal lithographic processes, 3D microfabrication using a novel sacrificial metallic mold (SMM), and other 3D methods involving polyimide as a mold and insulating material.

## 2. DESIGN

The design of inductors on a chip are dependent upon many factors. These factors include geometry, type of insulating material, number of turns, and type of conductor used.

Geometry plays an important role in the inductance. The width of the wire and spacing of wires determines the density of lines in the spiral planar inductor. Refer to Figure 1 below.

Figure 1: Define width and thickness of wire



This directly affects the number of turns ( $n$ ) in the design. The inductance increases by a factor of  $n^2$ . The thickness of the wire in conjunction with the width also affects inductance. This is due to flux created by magnetic fields.

Wires must also be insulated by a good insulator such as silicon oxide, or an air gap. The addition of a magnetic material between insulated wires will increase the inductance of the design. The quality factor ( $Q$ ) can be increased by choosing a conductor with low resistivity.

A total of ten inductors were designed in Mentor Graphics IC Station layout tool. All inductors were built on a 4-inch silicon substrate insulated by 5000Å of silicon oxide. The theoretical inductance values were designed to range from 17nH to 300nH. The theoretical equation used to calculate inductance was from a modified Wheeler Formula [3]:

$$L_{mw} = K_1 \mu_o \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad [3]$$

The values of  $K_1$  and  $K_2$  are constants, where  $K_1 = 2.34$  and  $K_2 = 2.75$ . These constants are dependent upon geometry. For this model, an inductor for a given shape is completely specified by the following: number of turns  $n$ , the outer diameter  $d_{out}$ , the inner diameter  $d_{in}$ , the average diameter  $d_{avg} = 0.5(d_{out} + d_{in})$ , or the fill ratio, defined as  $\rho = (d_{out} - d_{in}) / (d_{out} + d_{in})$ . The symbol  $\mu_o$  is the permeability of free space equal to  $4\pi \times 10^{-7}$  H/m.

Geometry and number of turns were varied to investigate the effects on inductance as stated above in the abstract. Refer to Table 1.1 below.

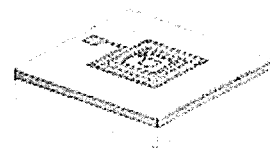
Table 1.1: Inductor designs

Inductor #	Line width (um)	Space Width (um)	(n) # of turns
1	5	5	15
2	10	5	15
3	10	10	15
4	10	15	15
5	10	20	15
6	15	5	15
7	20	5	15
8	10	5	5
9	10	5	10
10	10	5	20

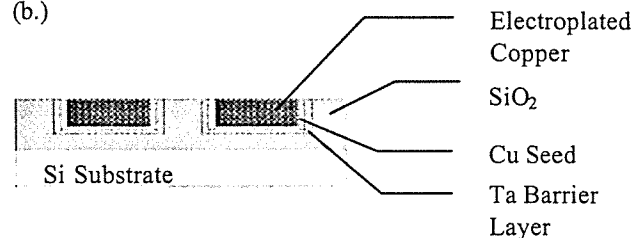
Copper was chosen as the conductive material. Thermal Silicon oxide two microns thick was chosen as the insulating material. A square spiral planar geometry was used for ease of layout and fabrication. Refer to figure 2a.

Figure 2: 3D Design and Cross Section

(a.)



(b.)

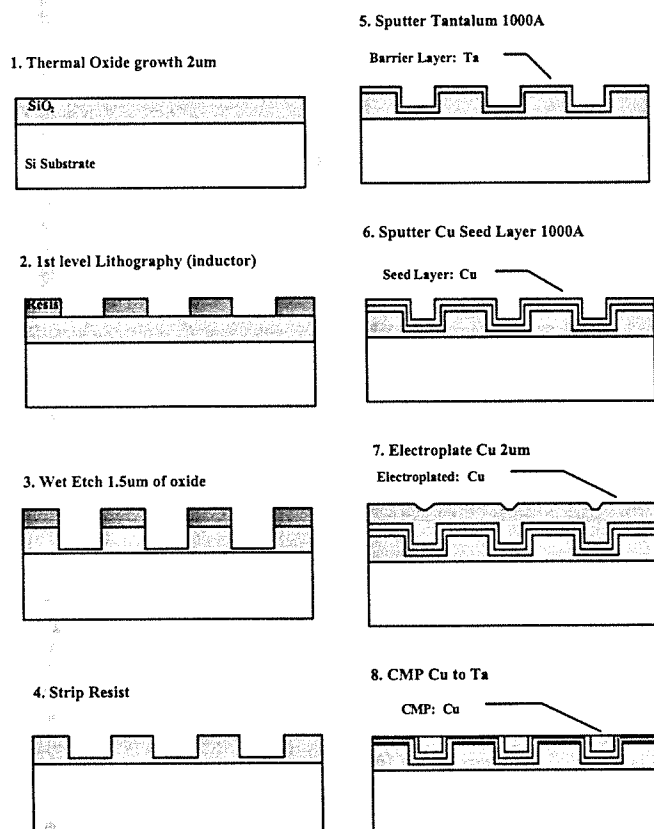


All inductors were designed with one level of metal to reduce amount of time for fabrication. The process used to fabricate the inductors designed in this project was a single copper damascene process.

## 2. PROCESS

The purpose of the process used in this project was to demonstrate a single copper damascene process and provide the groundwork for future research in the integration of inductors on a chip. With slight variation to the process used in this project, all designed inductors will be CMOS compatible. There are several key steps for the process used in fabrication of the designed inductors. These steps are deposition of insulating material, 1<sup>st</sup> level lithography, etching of insulator, deposition of barrier and seed layer, electroplating of copper, chemical mechanical planarization of copper, and electrical testing. The process steps will be described below. Refer to Figure 3 for process steps

Figure 3: Process Steps



### A. Thermal oxide growth

Approximately two microns of thermal silicon oxide was grown on a p-type substrate. This oxide was grown in the Bruce Furnace Tube 01 with recipe #420 20,000A wet field oxide. For demonstration purposes thermal oxide was chosen because it provided the best uniformity and control of thickness for the desired insulating material. To make the process CMOS compatible, other means of deposition of silicon oxide could be used. Some examples include LTO, or a PECVD oxide. It also can be noted that other insulating materials could have been used instead of silicon oxide. Some examples could be air, polyamide, or SU8.

### B. 1<sup>st</sup> level lithography

The 1<sup>st</sup> level lithography used in this process was RIT's standard one-micron resist recipe. The GCA1006 coat track was used to coat one micron of positive photoresist. All parameters were set the same as RIT's process. The GCA g-line stepper was used for exposure. A different stepper job was used to compensate for a slightly larger chip size. Development was completed on the GCA1006 development track. All parameters were identical to RIT's standard development program.

### C. Etching

Wafers were wet etched in BOE for 17.5 minutes. Wet etching was chosen to reduce the amount of processing time. The ideal etch would be an anisotropic plasma etch with an ICP power source. This process would require a deep UV curing step prior to etching, or a much thicker resist. After etching, resist was ashed, and RCA clean is necessary.

### D. Deposition of Barrier and Seed layer

Tantalum was chosen as the barrier layer. The thickness was 1000A. Next a 1000A copper seed layer was deposited. Both Ta and Cu were sputtered in a CVC601 sputter system. The base pressure reached in the system was 5E-6 torr. First a pre-sputter of Ta was conducted for 10 minutes followed by an 8 minute sputter. An 8-inch target was used for better uniformity across the wafers. Next, without breaking vacuum, copper was pre-sputtered for 10 minutes. This was followed by an 8 minute sputter of copper. The Cu target was also 8-inch. This process was developed by Deepa Gazula.

### E. Electroplating of copper

Copper electroplating was conducted on a Reynolds Tech electroplating system. The electroplating recipe used



was 2.50A for 5 minutes at a total of 12.5 A-min. The temperature of the bath was approximately 25°C and allowed to warm up for four hours. Wafers were plated one at a time. An o-ring was placed on back of wafer to help increase contact to electrode. This process was developed by Keith Udut

### F. Chemical Mechanical Planarization of Cu

CMP was conducted in the CMP lab on the tool designated for copper polishing. The CMP process used in this project was a two step process. All wafers were polished one at a time at the first step, then same procedure was followed for second step. The first step involved polishing with a fast removal rate slurry. The second step used a slower removal rate slurry. The faster slurry had a removal rate that was 10 times greater than the slower slurry. All copper except approximately 2000Å was removed with first slurry. The second slurry was used to remove the remaining copper. The purpose of the second slurry was to reduce the effects of dishing. Total process time was 48 minutes. This process was developed by Jeffery Perry.

### G. Electrical testing and characterization

Some electrical testing and characterization was completed for the devices. Resistance measurements were taken using analyzer 3. An LCR bridge was used to try and measure inductance with no success. Further testing on a network analyzer capable of measuring such small inductance is necessary in the future.

## 3. RESULTS

A single copper damascene process has been demonstrated in this project. Resistance measurements indicate that devices will work. Refer to table 2 for data.

Table 2: Resistance Measurements

Inductor #	Average Measured Resistance (ohm)	Theoretical Resistance (ohm)
1	79.67	64.200
2	76.63	37.596
3	68.77	43.080
4	74.53	48.108
5	72.53	53.304
6	69.07	28.960
7	64.13	24.462
8	21.13	9.480
9	43.57	21.960
10	120.00	57.720

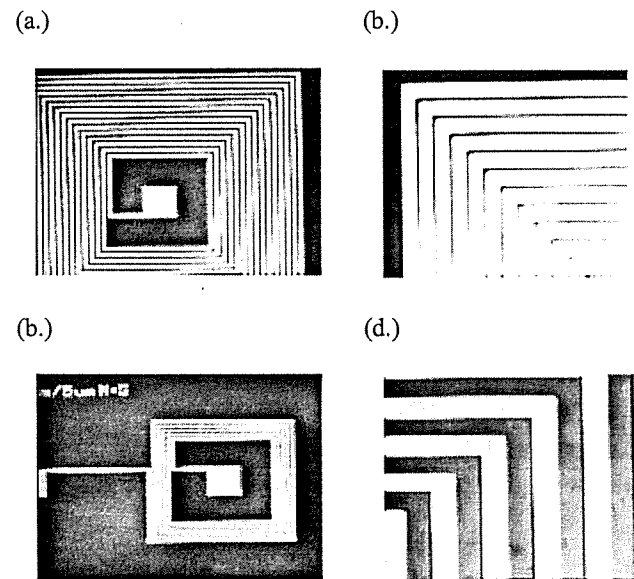
Measurement of inductance still needs to be completed to verify designs. Refer to Table 3 below for theoretical inductance values. Also quality factor needs to be measured.

Table 3: Theoretical Inductance using Modified Wheelers Equation

Inductor #	Line width (um)	Space width (um)	(n) # of turns	Lmw (nH)
1	5	5	15	155.34
2	10	5	15	159.65
3	10	10	15	167.15
4	10	15	15	176.34
5	10	20	15	186.52
6	15	5	15	167.74
7	20	5	15	177.69
8	10	5	5	17.74
9	10	5	10	69.06
10	10	5	20	297.67

Figure 4a – 4d are some microscope pictures of fabricated inductors. There are well-defined lines and spaces as can be seen in each figure. Refer to figures below.

Figure 4: microscope pictures of fabricated inductors



The next three pictures in figure 5 are SEM pictures of fabricated devices. It must be noted that samples were not prepared properly. These pictures provide a cross sectional view of a several lines, single line, and measurements of etch profile.

Figure 5: SEM pictures

(a.)

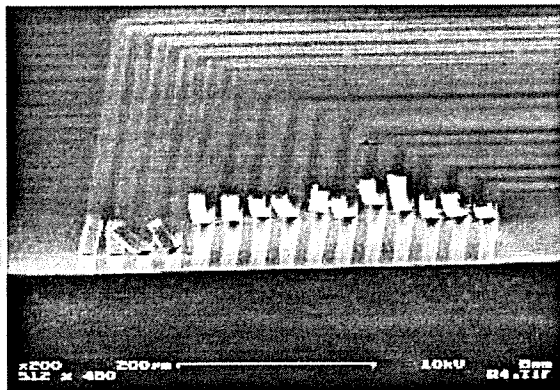
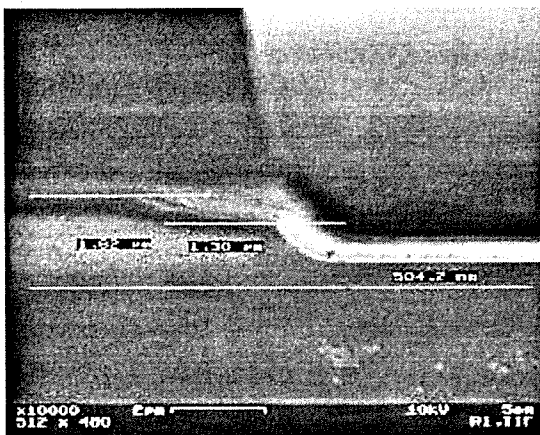
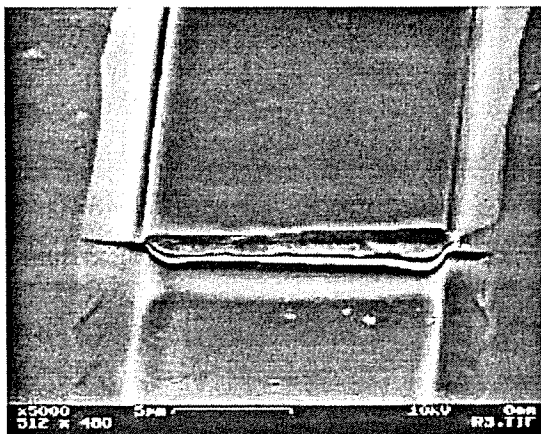


Figure 5: continued

(b.)



(c.)



## REFERENCES

- [1] David K. Cheng, "Fundamentals of Engineering Electromagnetics", Addison-Wesley Series in Electrical Engineering, Chapter 5-10, p. 201-214, 1993.
- [2] Christensen, K.T., "Easy Simulation and Design of On-Chip Inductors in Standard CMOS Processes", ISCAS '98. Proceedings of the 1998 IEEE International Symposium on Circuits and Systems (Cat. No.98CH36187), p. 6 vol. (xiv+603+489+874+615+557+656), 360-4 vol. 4 (1998).
- [3] Sunderarajan S. Mohan, Maria del Mar Hershenson, Stephen P. Boyd, and Thomas H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances", Vol. 34, no. 10, IEEE Journal of Solid-State Circuits, p. 1419-1424, Oct 1999.

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# Full-Wafer DMOS Fabrication at RIT

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**Abstract-** A well understanding of basic structure of Double Diffused Metal Oxide Semiconductor (DMOS) and the concept of segmented large capacitor creates possibility to produce a full-wafer DMOS. Using the Mylar Mask Technology, the final metal layer can be patterned accordingly so that to leave out any damaged fragments. Thus, it will increase the possibility of higher yield. Most of the basic fabrication processes will be done at RIT microelectronics lab facilities, and the functionality tests will be conducted at Naval Research Lab. Therefore, this paper is intended to give a general overview of concepts involved and the fabrication processes.

## 1. INTRODUCTION

Power MOSFET found its origin in the MOS integrated-circuit technology. Prior to the development of power MOSFET, the predominantly used high-speed power device was the power bipolar transistor. Although this type of power device provides needed characteristics, such as current handling capability of several hundred amperes and blocking voltages of several hundred volts, it has some major drawbacks.

First, the bipolar transistor has a complex and expensive base drive circuitry. Not only it needs large base drive currents to maintain the device in the on-state, but also requires even a larger base drive currents to obtain high-speed turn-off. Secondly, under the application of high current and voltage simultaneously, the bipolar transistor is prone to second breakdown failure mode. These disadvantages led to the development of power MOSFET technologies.

Unlike the bipolar device, no significant gate current is needed to operate in either the on-state or off-state condition. The control signal is done through induction process. A bias voltage is applied to the gate electrode that will effect the state of charge of the semiconductor that is separated by a thin layer of oxide. Furthermore, the power MOSFET also reduced the possibility of second breakdown failure. There are several structures of power MOSFET that have been thoroughly developed. In this project, however, only the vertical DMOS will be explored and used.

In order to obtain higher power handling capability, DMOS are usually constructed in repetitive pattern of small cells. This project will explore the possibility to construct a full-wafer of these DMOS cells. This device is expected to have current handling of several thousands amperes and blocking voltage of several thousand volts. The future application of the device will be used for mega Watt (~12 MW) Power Converters and Drivers for: utility power distribution, electric drive for ships, tanks, and locomotive, linear motors for air craft carrier launch and arrest.

## 2. BACKGROUND THEORY

### A. Introduction to Basic DMOS Structure

The basic structure of vertical DMOS is shown in Figure 1. N-type substrate is normally used because electrons, the majority carrier, have higher mobility, producing faster performance. The doping concentration of the substrate will determine the on-resistance of the device. In addition, the on-resistance can also be minimized by using wafer with (100) orientation because it provides the highest surface mobility.

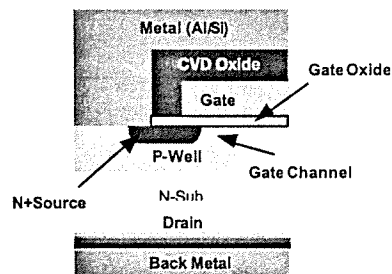


Figure 1. Basic Vertical DMOS Structure

As shown in Figure 1, the electrons path is vertical, from the source region that is on the top surface, to the drain region, which is the backside of the wafer. For this reason, the device is named vertical DMOS. The backside of the wafer is usually doped heavily to reduce the contact resistance thus minimizing the on-resistance.

The gate oxide quality is also of a great concern since the operation of the device is done by modulating an electric field across the gate oxide. Producing a defect-free gate oxide has been a major challenge, especially if it involves a large area, which is vulnerable to physical defects, such as pinhole and local oxide conglomeration.

The basic operation of DMOS is similar to the MOSFET technology. In order for the current to flow from drain to source, a path needs to be created in the p-well region to allow the flow of electrons from source to drain. For this to happen, a positive bias voltage is applied to the gate electrode that will repel the holes in the p-well region thus creating an n-channel that is the gate channel. If there is a potential difference between the drain and the source, current flows. In addition, the gate channel length is determined by the junction depth of p-well and n+source.

In the on-state condition, the source is grounded, and a positive voltage is applied to the drain. Assuming the channel exists, current will flow from drain to source. Unlike in the MOS integrated circuit, conduction is done by the majority carrier in the n-type substrate in power DMOS. It is important to note that the source and the p-well is shorted at all time to establish a fixed potential to p-well region during device operation. In the off-state condition, the gate electrode is grounded by short-circuit it to the source. By doing this, the conducting channel at p-well region is shut-off.

The robustness of the fabrication process will determine the electrical characteristics of the device. The following are some device parameters that are important to understand and can be used as a quantitative measure of how well the device was fabricated.

### 1. Forward Blocking Capability

To obtain this device parameter, the gate and the source is shorted, and a positive voltage is applied to the drain. As a result, depletion layer is formed at the p-well/n-sub junction. As the drain voltage increases, the depletion width also increases. When the depletion region reaches the n+source/p-well junction, breakdown occurs. In the DMOS structure, the doping profile and curvature are crucial in determining the forward blocking capability.

### 2. Threshold Voltage

Threshold voltage is the minimum bias voltage applied to the gate electrode at which a strong inversion begins to occur, creating the n-channel for current to flow.

### 3. On-Resistance

The on-resistance is the total resistance of the current path, from the drain to source. This parameter can be broken down to a series of smaller resistances: n+source, channel, junction, n-sub, and n+contact resistance. On-resistance is very important parameter because it determines the power rating of the device.

### B. The Concept of Segmented Large Capacitor

In order to understand the idea of full wafer DMOS, it is crucial to grasp the basic concept of segmented large MOS capacitor. The oxide layer is the primary concern in this matter. As it is understood, the dimension of the oxide will determine the capacitance. However, even more crucial than the dimension is the physical robustness of the oxide, such as defect density and pinholes. As illustrated in Figure 2(a), a single tiny pinhole will ruin the whole device because it will short-circuit the two electrodes.

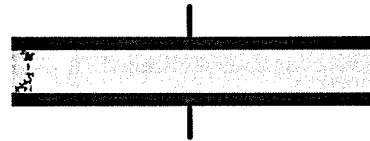


Figure 2. Oxide Defects in Large Capacitor

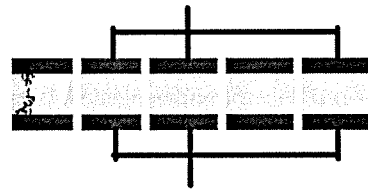


Figure 3. Segmented Large Capacitor

As a solution, the large capacitor is segmented into smaller capacitors; thus confining the defects to smaller areas. After testing the whole capacitors segments, good capacitors are then connected in parallel as shown in Figure 3. Therefore, the method will significantly increase the yield.

### C. Full-Wafer DMOS

In the same manner, the fabrication of a full-wafer DMOS is most likely to fail due to poor large gate oxide due to presence of particulates, defects, and pinholes. Adopting the idea of segmented large capacitor, this project will attempt to fabricate a full-wafer DMOS.

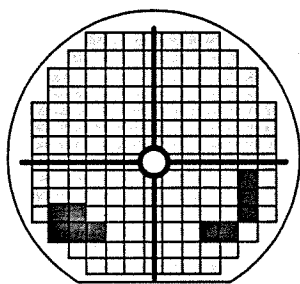


Figure 4. Full Wafer DMOS

The mask will be designed in such a way to repeat DMOS cells on the entire wafer. Prior to the last metal step, test will be conducted on each of the DMOS cell. The damaged cell will be marked, and using the mylar mask technology the final metal layers will be patterned in such a way to connect working devices. Figure 5 shows a wafer of the preliminary experiment with mylar mask.

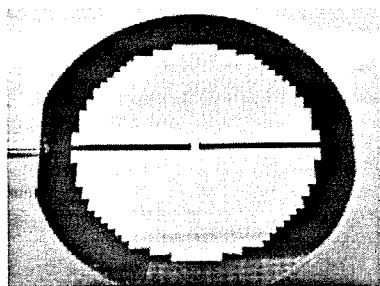


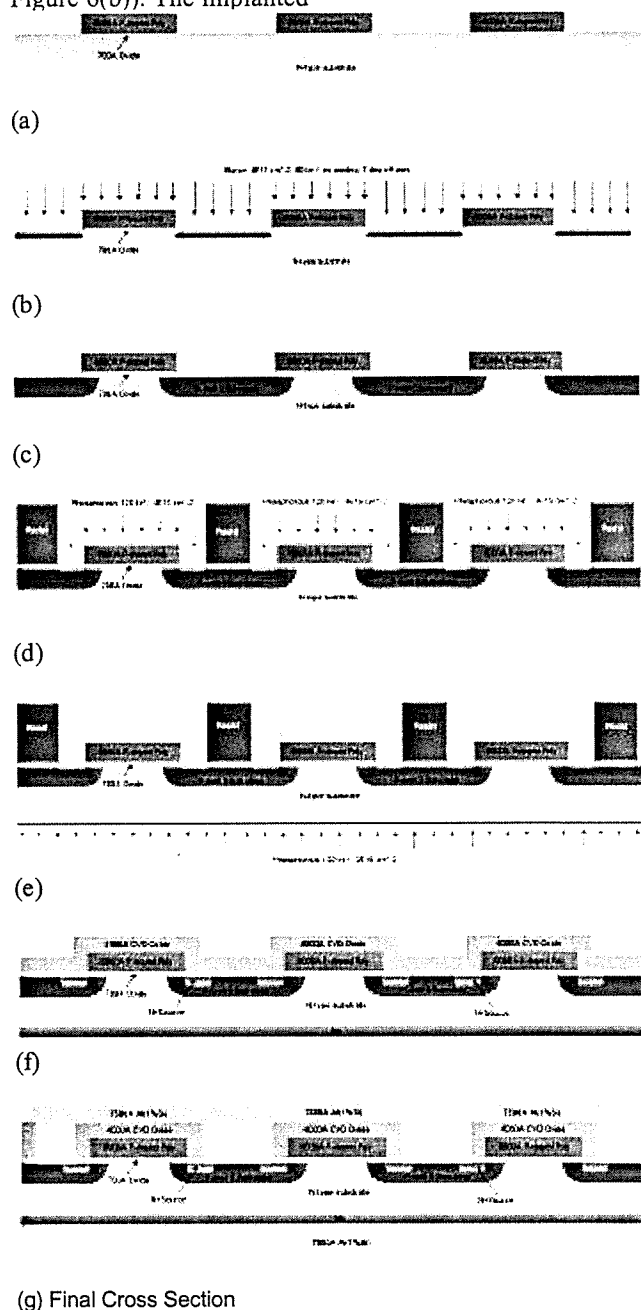
Figure 5. Preliminary experiment with mylar mask.

### 3. FULL-WAFER DMOS FABRICATION PROCESS

The full-wafer DMOS process was developed from an established RIT CMOS process. It involves four-level mask with the mylar mask as the last photo step. Figure 6 shows the cross sections and process flow of the fabrication process.

Four-inch N-substrate wafer with low resistivity and (100) crystal structure will be used. After proper cleaning procedure, 700 Å of gate oxide is thermally grown. A layer of 6000 Å of polysilicon is deposited on top of the oxide using LPCVD. The dopant concentration on the polysilicon then is adjusted by controlled phosphorous diffusion. The polysilicon then is patterned using standard procedure of photolithography into gate electrodes of the DMOS cells as illustrated in Figure 6(a).

Boron implant of 60 keV and dose of  $4 \times 10^{13} \text{ cm}^{-2}$  is done at 7 degree off axis to minimize channeling effect (see Figure 6(b)). The implanted



(g) Final Cross Section

Figure 6 Cross Sections of Full-Wafer DMOS. The drawing doesn't reflect the proper scaling.

boron then is annealed at  $1100^\circ\text{C}$  for 255 minutes at  $\text{N}_2$  ambient, forming the p-well region as shown in Figure 6(c). After this step, a layer of photoresist is applied on the front side of the wafer. This makes possible for the stripping of polysilicon at the backside of the wafer.

The next step is to form the n+source region. The second level of photolithography defines the area for

n+source as seen in Figure 6(d). Phosphorous implant of 120 keV and dose of  $4 \times 10^{15} \text{ cm}^{-2}$  s is done using cooling system at 7 degree off axis. Phosphorous is also implanted at the backside of the wafer at lower dose of  $2 \times 10^{15} \text{ cm}^{-2}$ . After annealing it at  $1000^\circ\text{C}$  for 20 minutes in  $\text{N}_2$  ambient, a  $1000 \text{ \AA}$  of oxide is thermally grown by wet oxidation. On top of the oxide layer,  $4000 \text{ \AA}$  of CVD oxide is deposited as an insulator layer between the poly gate and metal layer. To increase the oxide performance, it was annealed at  $900^\circ\text{C}$  for 30 min in  $\text{O}_2$  ambient (see Figure 6(e)).

As shown in Figure 6(f), the third photolithography step is to define the contact window. The next step is to deposit 7500 of aluminum with 1% of silicon using sputtering technique both at the front and back side of the wafer. The final metal layers then is patterned using the mylar mask technique. Figure 6(g) shows the final cross section of the device.

### ACKNOWLEDGMENT

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### BIBLIOGRAPHY

Baliga, B. Jayant, *Modern Power Devices*, Willey, NY, 1987.

## Reflection Transmission Modulator

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**Abstract—** Microelectromechanical systems (MEMS) have gained increasing importance in the semiconductor industry. The research done had three main goals. The first was to pattern a corrugated pattern in photoresist. The second was to obtain a variation in the stress of the materials used and the third was to fabricate a micro. The micro shutter is constructed using a stack consisting of Amorphous Carbon and Aluminum and is anchored at one end to the substrate. In this study two of the three goals were met however there were some difficulties with the fabrication of the micro shutter that will be discussed later on.

## 1. INTRODUCTION

MEMS has been a major interest in the semiconductor industry since the 1960's when Richard Feynman offered prize money for a micromotor and then came up with the fabrication process that used a sacrificial layer. By the 1990's MEMS had become an integral part of automotive, medical, and consumer applications to name a few.

MEMS is the marriage of computation and physical sensing and actuation. In short it is the combination of both electrical and mechanical components. This is beneficial because MEMS utilizes the same general processes used in microelectronics. The devices are miniaturized and can be produced in mass. One can even build IC devices and MEMS devices together on the same chip. Figure 1 shows the integration of the standard CMOS process and a MEMS cantilever.

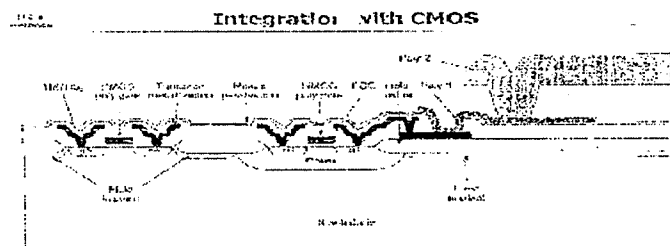


Figure 1: MEMS integration with CMOS

Most of the consumer applications use MEMS applications where the cantilever is corrugated. This corrugation in the cantilever is there to one, reduce the stiction between the cantilever and the substrate and two, allow the cantilever to curl in only one direction just like a piece of corrugated cardboard. The way that the dimple is formed is by depositing the metal and then etching into it to form the dimples. This project will explore patterning the cantilever by patterning the sacrificial material.

## 2. PROCEDURE

The work done on this project was completed in three major sections. The first was to obtain the corrugation in the resist. The second was to obtain different stresses in the materials of the cantilever and the third was to actually fabricate the device.

### A. Corrugation of sacrificial layer

The sacrificial layer used was positive photoresist with a thickness of about one micron. A Box-Behnken design of experiment was set up to generate runs that might yield the necessary corrugation.

Run #	Temperature Time (s)	Energy Time (s)	Force (mN)
1	2.0	4	2.5
2	1.0	2	2.0
3	1.0	2	2.5
4	2.0	4	2.5
5	1.0	2	2.5
6	1.0	2	2.5
7	2.0	4	2.0
8	2.0	4	2.0
9	1.0	2	2.0
10	1.0	2	2.5
11	2.0	4	2.5
12	2.0	2	2.5
13	1.0	2	2.0
14	3.0	6	2.0
15	1.0	2	2.5

Table 1: Design of Experiment Run order

### B. Stress Analysis

The cantilever that was fabricated for this project was done using a two level stack consisting of amorphous carbon on the bottom and aluminum on the top. The reason for using the two different materials is because they are deposited to have opposing stresses. The amorphous

carbon is compressive while the aluminum is tensile. The opposing stresses is what will cause the cantilever to curl up in the relaxed state.

The aluminum was deposited in the evaporator and the amorphous carbon was deposited in the Drytek Quad using the following recipe:

Time = 45 seconds  
CH<sub>4</sub> = 50 sccm  
Pressure = 100 mTorr  
Power = 300 watts

### C. Device Fabrication

Once a recipe was chosen for the corrugation of the sacrificial material and the proper stress measurements were obtained on the cantilever materials the device was ready to be fabricated. The procedure used to fabricate the device is found below.

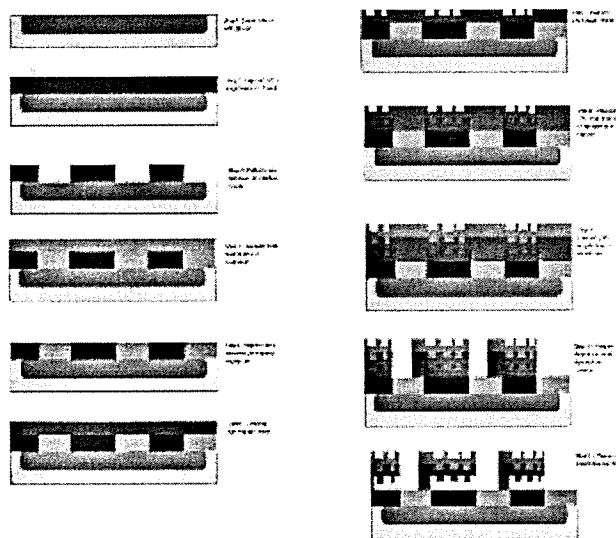


Figure 2: Reflection/Transmission Modulator Process Flow

### 3. RESULTS



Figure3: Too little corrugation (1)



Figure4: Too much corrugation



Figure5: Corrugation used in fabricating device

Figure6: Stress Analysis of Amorphous Carbon



Figure7: Failed Fabricated Device

Figure 3 shows one of the Design of Experiment runs that shows that corrugation was achieved but it was not enough. Figure 4 shows too much corrugation and figure 5 shows the recipe that was used in fabricating the device. Figure 6 shows what the measurements were from the stress analysis of the Aluminum and amorphous carbon. Figure 7 shows the picture of the failed device.

### 4. CONCLUSION

The reason this is called a reflection/transmission modulator is because this is one of the few optical MEMS devices that has the capability to both reflect light and allow it to be transmitted through. When the voltage is applied and the cantilever is extended light is reflected off the top surface. If the device were fabricated on top of a glass substrate when the device is in the curled state light can be transmitted all the way through.

This project shows that obtaining the corrugated pattern in the sacrificial material is possible and through the use of a design of experiment can be optimized so that the depth of the valleys in the corrugation are not so deep. When the resist corrugation has become ideal, the device should operate correctly.

### REFERENCES

- [1] Bozler, Carl (2000), Microelectro-mechanical system actuator device and reconfigurable circuits utilizing same. <http://www.delphion.com/cgi-bin/patsearch>. Patent# US6127908



[2] Bozler, Carl (1999) Spatial Light Modulator,  
<http://www.delphion.com/cgi-bin/viewpat.cmd/US05959763>  
Patent# 5959763.

[3] Bozler, Carl (1998) Spatial Light Modulator  
<http://www.delphion.com/cgi-bin/viewpat.cmd/US05784189>  
Patent# 5874189

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# Design and Analysis of a CMOS Based MEMS Accelerometer

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**Abstract—** Traditionally, microelectromechanical systems (MEMS) have been fabricated using standard surface micromachining or bulk micromachining processes with prior or subsequent CMOS incorporation. Recently, a new hybrid technique known as CMOS micromachining has been developed allowing for parallel fabrication of mechanical and electrical components. A single axis and dual axis accelerometer have been designed for submission for an ASIMPS alpha run using the CMOS micromachining process. Electrical and mechanical analysis and simulations for the single axis accelerometer have been performed. The sensitivity of the single axis accelerometer has been calculated to be 19.66mV/g neglecting the effects of parasitic capacitance. The released die has been packaged at RIT and a testing method has been determined and modeled.

## 1. INTRODUCTION

With the development of microelectromechanical systems, the ability to sense and actuate at the microscale level has been realized. Incorporation of electronic circuitry has allowed for mechanical signals to be converted to equivalent electrical signals providing information and an interface between electrical processing units and the outside world. Conversely, electrical signals can also be generated and converted into mechanical signals through the micromechanical components to thus act upon and influence the outside world. Because of the similar scale between integrated circuits and micromachined devices, IC processing technology has been adapted for the fabrication of the latter.

In general, two types of process have been used to manufacture microelectromechanical systems. The first type of process, known as surface micromachining, utilizes various thin films and a sacrificial layer, deposited and patterned on a silicon wafer to create the structural layers of the device. The sacrificial layer is then etched away, releasing the upper layers and creating a freestanding device. In contrast, bulk micromachining utilizes the thickness of a silicon wafer to create the micromachined structures. In a bulk micromachining process, a masking

layer is deposited and patterned on the silicon surface and the substrate is then selectively removed to create the micromachined structures. While each of these techniques lends itself to the fabrication of micromechanical components, the incorporation of the signal and control circuitry has had to be done off chip or with a prior or subsequent CMOS process.

Recently, a hybrid technique for fabricating MEMS devices, known as CMOS micromachining, [1] has been developed. With the CMOS micromachining process wafers are fabricated using any standard CMOS process. By devoting a section of the chip, void of electronics, the micromechanical structures are defined using the metal and dielectric layers for the CMOS interconnects. An anisotropic etch is then performed through the unmasked regions of the dielectric layers. Trenches are subsequently etched into the exposed substrate using a deep reactive ion etch (DRIE). An isotropic  $\text{SF}_6$  plasma etch is then used to remove the silicon underneath the metal and oxide interconnects thus releasing the mechanical components. The process flow is illustrated in figure 1.

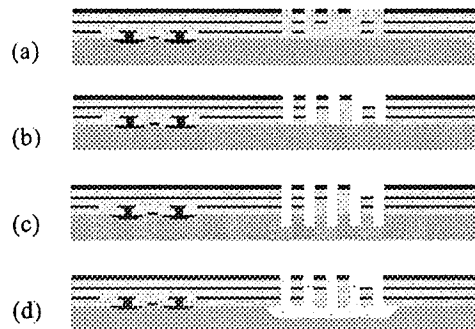


Figure 1: Illustration of the CMOS based MEMS process. (a) CMOS processed wafer. (b) Anisotropic oxide etch through the dielectric layers. (c) DRIE into silicon substrate. (d)  $\text{SF}_6$  release of metal/oxide structures.

In an effort to promote the fabrication of prototype MEMS devices, the Department of Advanced Research Projects Agency (DARPA) is partially funding foundry runs for the new CMOS process, allowing end users to design their own chips for fabrication. Using Cadence and specific design rules developed by Carnegie Mellon University [2] a single axis and dual axis accelerometer based on an adaptation of the ADXL series accelerometer by Analog Devices, Inc. were designed for the Fall 2000 Application Specific Integrated MEMS Processing Service (ASIMPS) alpha run.

## 2. DEVICE DESIGN

The ADI style accelerometer consists of three basic components as illustrated in figure 2. By using Newton's second law, which states that the force is equal to the product of the mass of an object and an applied acceleration, it is possible to detect an external acceleration through a measured force. In order to measure the force, two sets of interdigitated comb fingers, rotor and stator, are suspended from a proof mass supported by the mechanical springs and outer frame. The springs are designed to provide mechanical support for the suspended structure and to allow for the deflection of the proof mass in response to an applied acceleration. In turn, proof mass is designed such that a significant mass is present for response to an acceleration as well as providing an anchor point for the rotor fingers which form the electrodes of the parallel plate capacitors. Under an applied acceleration, the proof mass will deflect causing a change in capacitance between the stator fingers and the rotor fingers. Since capacitance is a measure of the electrical force, the mechanical energy in the system can be converted into an electrical signal representative of the magnitude of the acceleration.

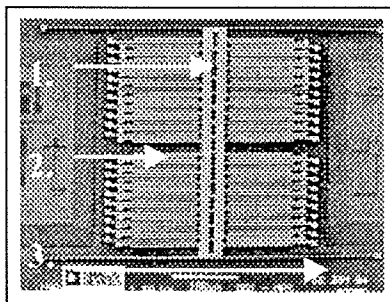


Figure 2: SEM of ADI accelerometer showing the proof mass (1), electrodes (2) and springs (3). [3]

The mechanical sensitivity of the device can be tailored, through the spring constant, by controlling the amount of deflection for a given mass and acceleration. In order to provide the maximum sensitivity for the device the distance between the stator fingers and the rotor fingers

should be minimized and the cross sectional area should be maximized. To ensure that the electrodes do not become electrically shorted under a large acceleration, the gap must be larger than the maximum deflection of the springs. Alternatively, grounded limit stops must be incorporated into the design such that the gap between the limit stops is slightly less than the electrode gap.

As part of the adaptation of the ADI accelerometer [4] which this design was based upon, an outer frame is utilized for the anchor point of the stator fingers in order to match the out of plane curl induced by thermal stresses in the bimorph structures of the released layers. Additionally, certain structures were designed in order to adhere to the MEMS design rules for the die submission. Ideally, the parasitic capacitances, consisting of the substrate to device capacitance, interconnect capacitance and bondpad capacitance, should be minimized.

By routing the electrical interconnects through the mechanical structures using the first and second metal layers, a full capacitive bridge can be realized. Two input signals, 5V pulsed waves at a frequency of 1MHz, are applied 180 degrees out of phase. The signals are applied to every other movable electrode by routing the electrical signal through the springs and proof mass. The output signals, positive and negative, are extracted from the fixed electrodes. Figure 3 shows a detail of the electrode layout as well as the equivalent circuit model.

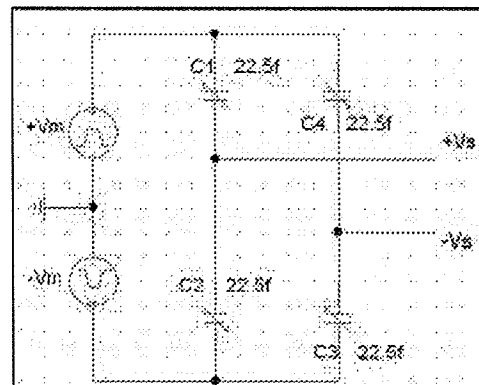
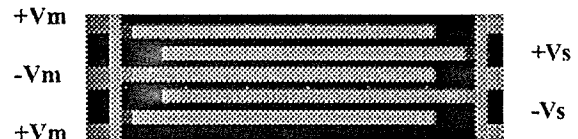


Figure 3: (a) Electrode layout and signal designation. (b) Equivalent circuit model.

### 3. MODELING

#### A. Mechanical Modeling

A simplified mechanical model for the spring system can be obtained by treating each beam as a simple cantilever and using force methods to extract the spring constant. In this analysis it is assumed that the effects of the trusses in each spring are negligible. Using Hooke's Law for a single cantilever, the spring constant can be defined as

$$k = F / \delta \quad (1).$$

Substituting the displacement as function of force gives the spring constant for a single beam in the spring system as

$$k = \frac{3EI}{l^3} \quad (2),$$

where E is Young's Modulus of the material and I is the moment of the beam in the z direction, given by

$$I = \frac{wh^3}{12} \quad (3).$$

Since each spring consists of four beams, the spring constant becomes one quarter of the individual spring constant. The entire spring system consisting of four sets of springs is then four times the spring constant of each spring set which can be expressed as follows

$$k = \frac{E(wh^3)}{4l^3} \quad (4).$$

A more advanced model, which takes into account the effects of the trusses on the spring constant, was derived by Fedder [5] using energy methods. By applying Castigliano's second theorem to the individual components of each spring an equation for the overall spring constant of the system was found to be

$$k = \frac{48EI_b[(\tilde{a} + l_b)n - l_b]}{l_b^2(n-1)[(3\tilde{a}^2 + 4\tilde{a}l_b + l_b^2)n - l_b^2]} \quad (5),$$

where n is the number of trusses in each spring,  $l_b$  is the length of the beam and  $\tilde{a}$  is given by the ratio of the beam moments

$$\tilde{a} = \frac{I_b l_t}{I_t} \quad (6).$$

By taking the limit of equation 5 as  $\tilde{a}$  goes to zero, it can be shown that equation 5 is four times larger than equation 4. Closer analysis suggests that the constant factor in equation 5 should be changed to 12 giving the spring constant for the system

$$k = \frac{12EI_b[(\tilde{a} + l_b)n - l_b]}{l_b^2(n-1)[(3\tilde{a}^2 + 4\tilde{a}l_b + l_b^2)n - l_b^2]} \quad (7).$$

#### B. Electrical Modeling

Since each capacitor in the full bridge will change as a function of the gap distance, the capacitance can be written as [6]

$$\Delta C = \frac{\epsilon A}{g_o \pm y} = \frac{\epsilon A}{g_o(1 \pm \frac{y}{g_o})} = \frac{\epsilon A}{g_o} (1 \pm \frac{y}{g_o}) \quad (8).$$

By applying Kirchoff's Current Law in the frequency domain at the positive output of the half bridge circuit, an expression for the output voltage can be expressed by

$$V_s = \frac{sC_1 - sC_2}{sC_1 + sC_2 + sC_p + \frac{1}{R_l}} V_m \quad (9).$$

The sensitivity of the device can then be found by substituting C1 and C2 with the proper sign from equation 8 and realizing that the displacement, y, can be expressed as the ratio of the force to the spring constant giving

$$\frac{V_s}{a} = \frac{2C_o}{2C_o + C_p + \frac{1}{R_l}} \frac{m}{kg_o} V_m \quad (10).$$

### 4. ANALYSIS AND SIMULATIONS

For the single axis accelerometer, the spring geometry which ultimately affects the spring constant can be found in table 1.

Table 1: Spring geometry

	Height	Width	Length
Beam	2.25um	2um	120um
Truss	2.25um	2um	4um

Using this geometry and a Young's Modulus of 61GPa [2] the spring constants were calculated using the force method (equation 4), the energy method (equation 5) and

the corrected energy method (equation 6). The results for the analysis of the spring constant are summarized in table 2.

Table 2: Spring Constant results

Method	K (N/m)
Force	0.159
Energy	0.505
Energy (Corrected)	0.122

IDEAS finite element analysis was performed in order to verify that the above spring constants were accurate. A solid model was constructed and a boundary condition was applied to the fixed end of the spring so that all motion was constrained. At the free end of the beam, a 1uN load was applied in the x direction. A plot of the displacement, shown in figure 4, was obtained. By noting the total displacement (28.2um) at the end of the spring, the spring constant was determined from equation 1. The resulting spring constant for the four spring set of 0.141N/m agreed well with the force model and corrected energy model. Because of the relative agreement between the three spring constants, the midpoint value of 0.141N/m was chosen for later calculations.

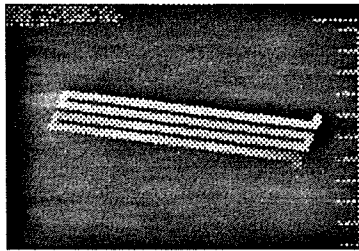


Figure 4: IDEAS FEA simulation results

For the 45um by 1.37um electrodes separated by a distance of 1.5um, the initial capacitance was calculated to be 19.25fF. The effective mass was calculated from the sum of the oxide mass of the rotor fingers and plate mass and the metal mass of the rotor fingers and plate mass. From equation 10, the sensitivity of the half bridge circuit with a 1GΩ load resistor was found to be 9.83mV/g neglecting the parasitic capacitance. For the entire bridge circuit the sensitivity was found to be 19.66mV/g.

Using PSpice, the full bridge circuit was simulated with a 1GΩ load resistor on the output from the positive and negative signal. A capacitive change of 0.37fF, corresponding to a 1g acceleration was simulated. The peak output of 186mV showed good correlation between the theoretical sensitivity and the output at 1g. Figure 5 shows the resulting waveform from the PSpice simulation. It should be noted that the decreasing output for each cycle

is most likely due to the capacitors charging. Ideally, the output from each node should be fed into a switched capacitor op-amp so that charging effects are minimized.

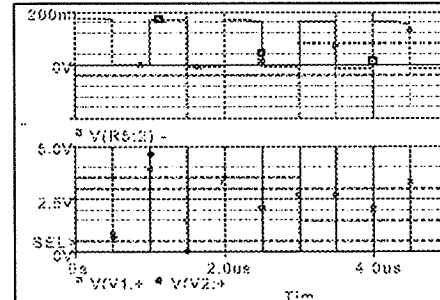


Figure 5: PSpice results for 1g acceleration.

## 5. TESTING METHODOLOGY

In order to test the device, the chip (figure 6) was packaged in a dual in-line package. Although no electrical tests were performed due to time limitations, a testing method has been developed. By placing the packaged chip at the end of a stainless steel cantilever beam, a time varying acceleration can be applied by deflecting the beam and allowing it to freely vibrate.

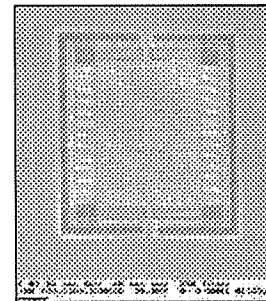


Figure 6: SEM of fabricated single axis accelerometer.

Simple vibration theory, which neglects the effects of damping, can be used to derive a theoretical equation for the acceleration. For a given beam, the deflection as a function of time can be expressed by

$$x(t) = x_0 \cos(\omega_n t) \quad (11),$$

where  $x_0$  is the initial displacement and  $\omega_n$  is the natural frequency of the beam. Taking the first derivative of the displacement with respect to time yields an equation for the velocity as a function of time give by

$$\dot{x}(t) = -\omega_n x_0 \sin(\omega_n t) \quad (12).$$

Taking the second derivative of the displacement with respect to time gives the time varying acceleration expressed as

$$\ddot{x}(t) = -\omega_n^2 x_o \cos(\omega_n t) \quad (13).$$

For a stainless steel beam 25cm x 3cm x 0.5cm, the peak acceleration corresponds to approximately 0.5g. The time varying acceleration is plotted in figure 7.

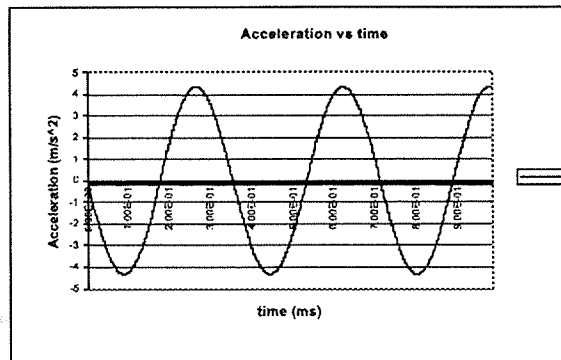


Figure 7: Time varying acceleration for a cantilever test structure.

For the actual device, it would be expected that the detectable acceleration would be significantly smaller than the theoretical results suggest. Since parasitic capacitances and the effects of curl were neglected in the analysis, the sensitivity of the device would be much lower than the calculated values. Additionally, the use of a resistive load will quickly cause a DC bias to form resulting in a damped output. A switched capacitor op-amp, donated by Mike Lu, was fabricated on chip and the outputs of one of the single axis devices were fed into the circuit. Although analysis was not performed on this circuit it would be expected that many of the problems associated with a resistive load would be alleviated yielding a working device.

## 6. CONCLUSIONS

A single axis and dual axis accelerometer were designed using the CMOS micromachining process. Careful modeling of the electrical and mechanical components demonstrated the ease of integration of two such systems at the theoretical level. Analytical evaluation of the single axis device showed good correlation with simulated results. A testing method, along with theoretical models has been presented and discussed. Future work includes analysis of the dual axis device in an analogous fashion, optimization of the test apparatus and testing of the device.

## REFERENCES

- [1] G.K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F. Guillou, M.S.-C. Lu, and L. R. Carley, "Laminated High-Aspect-Ratio Microstructures in a Conventional CMOS Process", *Proceedings of the IEEE Micro Electro Mechanical Systems Workshop*, San Diego, CA, Feb. 11-15 1996, pp. 13-18.
- [2] G.K. Fedder, K.J. Gabriel and T. Mukerjee, "CMOS-MEMS Design for the Application Specific MEMS Process Service (ASIMPS)", presented at Carnegie Mellon University, Pittsburgh, PA, July 2000.
- [3] <http://www.coyotesystems.com/products/products.9.html>
- [4] H. Luo, G.K. Fedder and L. Richard Carley, "A 1 mG Lateral CMOS-MEMS Accelerometer", in *The 13th Annual International Micro Electro Mechanical Systems Conference* Miyazaki, Japan, Jan 23-27, 2000, pp. 502-507.
- [5] G.K. Fedder, "Simulation of Microelectromechanical Systems", Ph.D. dissertation, EECS, U. C. Berkeley, 1994.
- [6] Y. Zhou, "Layout Synthesis of Accelerometers", M.S. thesis. Carnegie Mellon University, Pittsburgh, PA, 1998.

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# Characterization of SU-8 5 for MEMS Applications

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**Abstract**— SU-8 is a negative photoresist that is mainly used for MEMS technology. It is currently being used for micro-machined gears, accelerometers, and host of other MEMS structures. In these types of MEMS devices it is important to get an image with nearly vertical sidewall angles. For example with a micro-machined gear, the gear would slip easily if the gears sidewall angle not near vertical. The focus of this project was to model the sidewall angle through a designed experiment and an ANOVA was run on the data using a computer program. Also, using a linear regression analysis the functionality of the sidewall angle is determined within the specified design space. The design space for the main design was set up by using testing and screening experiment where the all the factors were set to the high levels and low levels of the design for feasibility of the main design. The sidewall angle was obtained by using Scanning Electron Microscope to view the cross-section of the samples in the DOE.

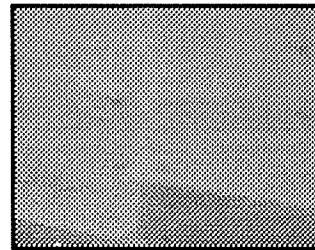
## 1. OPTIMUM PROCEDURES

First the wafers were scribed with the date and the tc of the designed experiment. Then the wafers were baked at 200 degrees Celsius for 30 minutes. Then a quarter size of SU8 5 was hand dispensed using a plastic cup. Then spin the spinner a 800-rpm's for 60 sec. Then spin the spinner for 5 minutes at 500 rpm. Next is a 55-degree celcius bake in a convention oven. It is important in this step to the wafer suspended in the convention oven meaning only a small portion of the wafer is touching something. This step allows the resist to flow and reduce the edge bead and planarize the resist. Next a softbake is down at 90 degrees Celsius for 5 minutes and 40 sec. It is important to make sure that the all hotplate are level so the resist when it flows it will not make the films uniformity get worse when it is on the hotplate. The exposure was done a 536 mJ/cm<sup>2</sup> on a Karl Suss contact aligner. Then the do a post exposure bake for 15 minutes at 90 degrees celcius. Next let the wafer sit on a clean room wipe to allow the wafer to cool. Now do a development with SU8 developer for 5 minutes at room temperature. Next a Phillips SEM was

used to take the pictures and a protractor was used to measure the angle.

## 2. RESULTS AND ANALYSIS

Just to illustrate what was actually measured with the sidewall angle a sample SEM picture is shown below:



**Figure 1:** This is a picture Oe3 which has a sidewall angle of 77 degrees.

The following sidewall angle data was collected using a Phillips SEM and is found below:

Run #	tc	Softbake (Sec.)	PEB (Sec.)	Develop (Sec.)	Sidewall (°)
3	( c )	260	690	385	74
5	a	340	690	215	82
7	b	260	1110	215	74
1	ab( c )	340	1110	385	85
6	Oe1	300	900	300	77
4	Oe2	300	900	300	79
2	Oe3	300	900	300	77

**Table 1:** This was the data used for statistical analysis and this shows that a 85 degree sidewall angle was achieved.

The data from the DOE was run on RS/1 which is statistical software. The first ANOVA was run with softbake time, PEB time, and develop time and the only factor that was to be found significant was the softbake time. So a second ANOVA was done with just the softbake time to get a better estimate of the residual. A

linear regression was then done to obtain the (1) found below:

#### Least Squares Coefficients

Term	Coeff.	Std. Error	T-value	Signif.
1 I	78.571429	0.461807		
2 ~S	4.750000	0.610913	7.78	0.0006

No. cases = 7    R-sq. = 0.9236    RMS Error = 1.222  
Resid. df = 5    R-sq-adj. = 0.9083    Cond. No. = 1

From this analysis it shown that 92.36% in the variation in the sidewall angle was coming from the softbake time. The significance value of 0.00006 so that there is 99.94% confidence level that the softbake time is controlling the sidewall angle with a linear relationship. Also, a t-test was done with the 3 center-points and the  $2^{3-1}$  fractional factorial design. By doing this t-test it was found that there was no curvilinear relationship between the softbake time and the sidewall angle. Also from this analysis the linear equation relating the softbake time with the sidewall angle is found below:

$$Y = 78.571429 + ((S - 300) * .11875)$$

In this equation Y stands for the sidewall angle in degrees and the S stands for softbake time in seconds.

## 5. CONCLUSION

The goal of the experiment was to test the hypothesis that the softbake time, Post Exposure Bake (PEB) time, and Develop time was a function of the sidewall angle. To test the hypothesis a  $2^{3-1}$  fractional factorial design was used and RS/1 was used to perform the statistical analysis. The softbake time accounted for 92.36% of the variation in the sidewall angle with 99.94% confidence in the data. The linear equation for the sidewall angle (Y) is  $Y = 78.571429 + [(S - 300) * 0.11875]$  where S is the softbake time in seconds. This equation is valid when S is between 260 seconds – 340 seconds at 90°C, the PEB time is 15 minutes at 90°C and the develop time is 5 minutes at room temperature. With this equation the predicted sidewall angle within the design space is 83.32°. If this equation is extrapolated outside of the design space, the predicted softbake time for vertical sidewalls is 6 minutes 36 seconds at 90°C, the PEB time is 15 minutes at 90°C and a develop time is 5 minutes at room temperature.

## REFERENCES

- [1] James R. Sheats and Bruce W. Smith, "Microlithography, Vol. 1-Science and Technology", Marcel Dekker Inc., NY, Chapter 9, 1998.

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